

Pre-Lab***NMOS Logic Gates***

1. In this laboratory exercise, you will use ZVN2110 MOSFET. Find and download the datasheet for this component.
2. Design and simulate a two input logic OR gate using three NMOS transistors. Use a 5 V logic level, allow the logic inputs to drive the gates of the transistors, and select the ZVN2106 transistor (compare how this is similar/different from the ZVN2110). Verify the proper logic function truth table with your simulation.

Laboratory Work

1. Build your two input logic OR gate using the ZVN2110 transistors. Limit current through each transistor to no more than 50% of its rated value.
2. Experimentally verify the proper logic function truth table of your circuit.
3. Experimentally determine and record the rise time, fall time, low-to-high output transition time, and the high-to-low output transition time. You may wish to save an oscilloscope screen capture for use in each of these measurements. Hint: use the function generator as the logic input signal and the single-shot triggering of the oscilloscope to facilitate accurate evaluation of these transitions.