

***Pre-Lab******CMOS Logic Gates***

1. In this laboratory exercise, you will use both the ZVN2110 and ZVP2110 MOSFETs. Find and download the datasheet for the PMOS transistor.
2. Design and simulate a two input logic OR gate using combinations of NMOS and PMOS transistors forming a CMOS structure. Use a 5 V logic levels, allow the logic inputs to drive the gates of the transistors. Verify the proper logic function truth table with your simulation.

***Laboratory Work***

1. Build your two input logic OR gate using the ZVN2110 and ZVP2110 transistors.
2. Experimentally verify the proper logic function truth table of your circuit.
3. Experimentally determine and record the rise time, fall time, low-to-high output transition time, and the high-to-low output transition time. You may wish to save an oscilloscope screen capture for use in each of these measurements. Hint: use the function generator as the logic input signal and the single-shot triggering of the oscilloscope to facilitate accurate evaluation of these transitions.
4. Compare the results of utilizing a CMOS implementation for this logic function versus an NMOS alone approach.