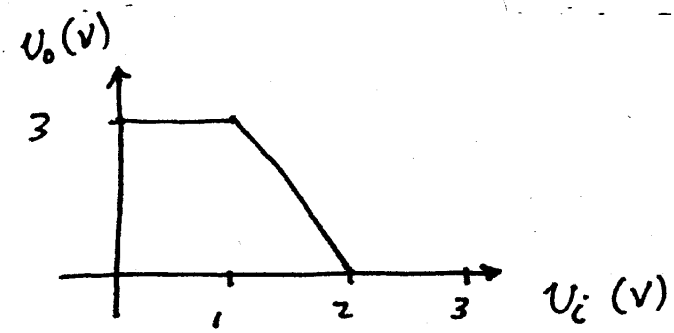
GIVEN:

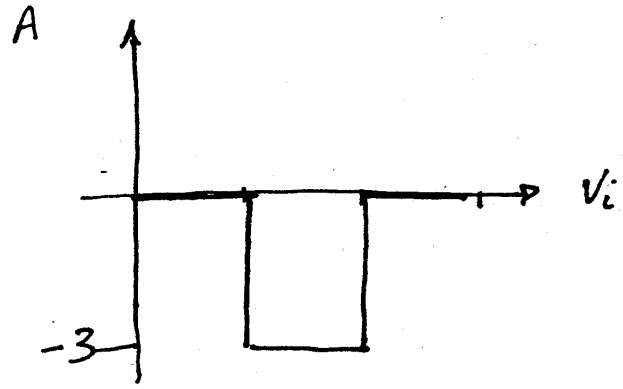


FIND: V_H, V_L, V_{IH}, V_{IL} PLOT $A_v = \frac{dv_o}{dv_i}$

SOLN:

$V_H = 3V$ $V_L = 0V$

$V_{IH} = 2$ $V_{IL} = 1$



TOPS 35500

GIVEN: 1 GHz PROCESSOR 10^9 GATES

AVE. PROP. DELAY = 150 ps 50W DISSIPATION

FIND: $P_{AVE,GATE}$ w/ 33% DUTY CYCLE

PDP

SOLN: $$P_{AVE,GATE} = \frac{50\,W}{10^9\,(0.33)} = 152\,nW/GATE$$

$$PDP = (150\,ps)(152\,nW/GATE) = 2.3\times10^{-17}\,J$$

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GIVEN: GRAPH OF FIG. P6.12

FIND: V_H, V_L, t_r & t_f FOR V_i & V_o

τ_{PHL} τ_{PLH} τ_p

SOLN: $V_H = 2.5V$ $V_L = 0.25V$

FOR t_r & t_f NEED TIME FROM 10% TO 90% & VICE VERSA ...

FOR V_o ... NEED t_r FOR 0.275 TO 2.25 V

$t_r \approx 10ns$ $t_f \approx 2ns$

FOR V_i $t_r \approx t_f \approx 1ns$

FOR τ_{PHL} NEED TIME FROM 50% V_i ($L \to H$) TO 50% V_o ($H \to L$)

$\tau_{PHL} \approx 1ns$

$\tau_{PLH} \approx 5ns$

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = 3ns$$