

3 November 2011

**United States Naval Academy
Electrical and Computer Engineering Department**

EC262 – Exam 2

1. Do a page check now. You should have 9 pages (cover & questions).
2. Read all problems in their entirety. Answer the question asked.
3. Work neatly and *show all of your work* to receive maximum partial credit.
4. Explicitly state any assumptions and *highlight your final answer*.
5. You have 110 minutes to complete the examination.
6. When directed by your instructor, you may commence work.
7. No calculators are permitted.

I will not discuss this exam with anyone until Friday 4 November 2011.

_____ (Signature)

Page	Points	Possible
1		
2		14
3		16
4		14
5		16
6		7
7		15
8		13
9		5
TOTAL		100

Name: _____ **Section** _____

1. [14 pts] Show a state diagram for a Mealy system with one input, x , and one output, z , such that $z = 1$ if and only if the input has been exactly two 1's followed immediately by exactly two 0's followed by exactly one 1. (Full credit for a system with 7 states.)

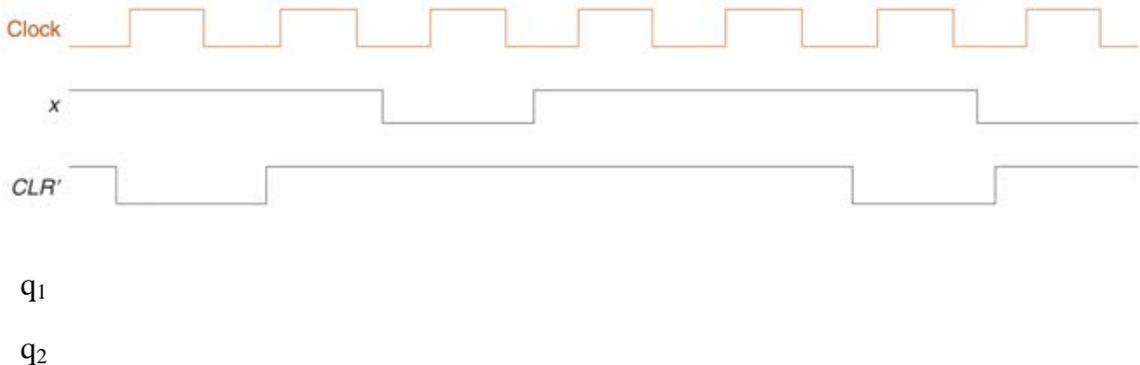
2. [16 pts] For the following state table and state assignments,

q	q*		z	
	x = 0	x = 1	x = 0	x = 1
A	D	C	0	0
B	B	A	0	1
C	B	D	1	1
D	A	B	1	1

q	q ₁	q ₂
A	0	0
B	0	1
C	1	1
D	1	0

a. [10 pts] Design the system using JK flip flops. Show the flip flop input equations and the output equation. You do not need to draw the circuit.

b. [6 pts] Complete the timing diagram below. Assume that the JKFFs are trailing-edge triggered flip flops.



3. [14 pts] For the following state table,

q ₁ q ₂	q ₁ * q ₂ *		z
	x = 0	x = 1	
0 0	1 1	0 1	0
0 1	0 0	1 1	1
1 1	1 1	0 1	0
1 0	X X	X X	0

a. [10 pts] Design the system using D flip flops. Show the input equations to the flip flops and the output equation. Do not draw the circuit.

b. [4 pts] Assume that the system initially starts at state 10, fill in the next states in the table below.

q ₁ q ₂	q ₁ q ₂ *		z
	x = 0	x = 1	
1 0			0

6. [22 pts] In an attempt to keep midshipmen awake, USNA will be installing vending machines around the campus intended to sell caffeine pills. Each caffeine pill will cost 15 cents. You have been asked to develop the controller for the vending machine.

Here are the specifications from the manufacturer:

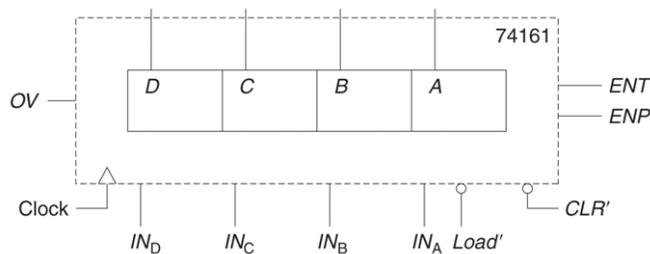
- The machine only accepts nickels and dimes (no pennies, no quarters, no weird Sacagawea dollar coins, etc.) Assume that the machine automatically returns any coin other than a nickel or a dime.
 - The machine's slot only accepts one coin at a time.
 - After the machine receives 15 cents, it dispenses one caffeine pill and five pages of safety directions (but, strangely, no water).
 - In an effort to squeeze money out of midshipmen, the machine does not give change. So, if a midshipmen deposits two dimes (or two nickels and then a dime), he gets his caffeine pill, but no change.
 - The manufacturer has already designed a circuit that resets the machine between customers, so you do not need to worry about this; assume that after a pill is dispensed, the machine resets for the next customer.
- a. [7 pts] Model the vending machine controller as a finite state Moore machine. Draw a state diagram (Hint: you should have 4 states).

b. [7 pts] Design the state transition table for the finite state machine.

c. [8 pts] Using K-maps, design an implementation for your controller using D flip flops. (Equations only).

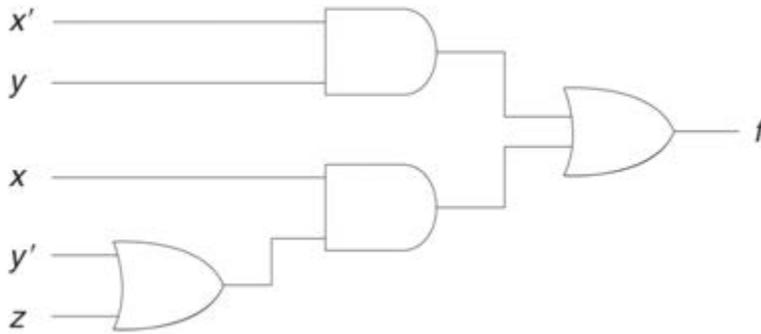
7. [5 pts] Draw a block diagram of a system that has an output of 1 when the input has been 1 for exactly 4 clock cycles followed immediately by exactly three 0's. Use only combinational logic gates and one 8-bit shift register.

8. [8 pts] Using combinational logic gates and 74161 counters, draw a circuit that outputs a clock pulse for every **eighteenth** input clock pulse. The block diagram of a 74161 counter is shown below.



- The lines labeled *D*, *C*, *B* and *A* are the outputs of the counter, with *A* as the LSb.
- The lines labeled *Clock* and *CLR'* are self-explanatory.
- The line labeled *OV* is the Overflow indicator, and is active when the counter output is 1111.
- The lines labeled *IN_D*, *IN_C*, *IN_B*, *IN_A* are used in conjunction with the *Load'* signal to load initial data into the counter (as a start value) if desired.
- The *ENT* and *ENP* are enable signals and must both be 1 for normal counting.

9. [5 pts] Complete VHDL code below to implement the following circuit.



```
1  LIBRARY IEEE;
2  USE IEEE.STD_LOGIC_1164.all;
3
4  ENTITY exam2_problem9 IS
5
6  PORT (
7
8
9
10
11  );
12
13  END exam2_problem9;
14
15  ARCHITECTURE combinational OF          IS
16
17  BEGIN
18      -- Implement function f here
19
20
21
22
23
24  END combinational;
25
```