Lab #3 **EC262**

PRE-LAB

1. Show a truth table for a full adder (FA) (including a C_{in} bit).
2. Using K-map technique, develop the minimum SOP expressions for the *Sum* and C_{out} bits.
3. Draw a logic circuit for the full adder.

LAB

1. Implement the full adder with Quartus.

2. Simulate the full adder using the QSim simulator and verify correct operation (functional simulation). Be sure to simulate all 8 possible input combinations.

3. Implement a 4-bit adder as shown in Figure 1.

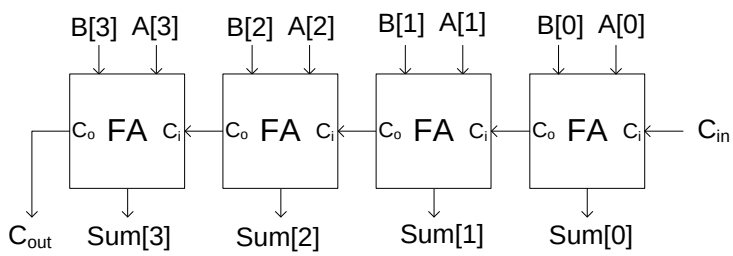

Fig. 1. Block diagram of a 4-bit adder

Note: you can create a symbol for a full adder and then use four of those adders to complete this task. Look at step VII in the tutorial "Quartus II Introduction " for instructions.

4. Simulate the 4-bit adder using QSim simulator and verify correct operation (functional simulation). Your simulation should include these inputs:

A in decimal	**B in decimal**	**Cin**
0	0 7 15	0
9	0 7 15	1
15	0 7 15	1

Note: you may need to edit the end time of the simulation to include all inputs. From QSim window, open or create a new simulation input file, then select **Edit > Set End Time…**

Print and attach the simulation results to your lab notebook.

5. Implement and program the 4-bit adder on the Altera board. Assign inputs and outputs of the adder as:

Inputs	**Switches**	**Outputs**	**Red LEDs (LEDR)**
Cin	SW0	Sum_0	LEDR0
A_0	SW1	Sum_1	LEDR1
A_1	SW2	Sum_2	LEDR2
A_2	SW3	Sum_3	LEDR3
A_3	SW4	Cout	LEDR4
B_0	SW5		
B_1	SW6		
B_2	SW7		
B_3	SW8		

Verify correct operation and demonstrate your design to your instructor.