Lab #6 **EC262**

PRE-LAB

1. Draw a block diagram for a 4-bit register that has the following characteristics:
    a. Using 4 D Flip Flops (DFFs),
    b. Rising/leading edge triggered,
    c. Active low *clear* signal
    d. No *preset* signal.

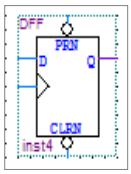

Fig.1. Symbol for a DFF

2. Design and draw block diagram for a 4-bit up counter (*Count* = 0_{16} to F_{16} and repeat). The value of the count should be displayed on a seven segment display. Assume that the following components are available:
    - Any logic gates or building blocks we have covered.
    - 4-bit adders from lab 3.
    - 4-bit registers (from #1).
    - Seven segment display driver from lab 4.

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LAB

In this lab, you will implement a 4-bit up counter on a DE2 board using a 4-bit adder (lab 3), a 4-bit register (prelab), and a seven segment display driver (lab 4).

1. Create a new project (in a new directory/folder) and implement a 4-bit register from PRE-LAB #1. Use 4 dff components from the Quartus library.

2. Compile, simulate and verify the 4-bit register.

3. Create a symbol for the 4-bit register (to be used later).

4. Copy and paste the block diagram/schematic files (.bdf files) of a full adder and a 4-bit adder from lab 3 to this lab directory. Add these files to your project (Project > Add Remove Files in Project).

5. Copy and paste the vhdl file (.vhd file) of a seven segment display driver from lab 4 to this lab directory. Add this file to your project (Project > Add Remove Files in Project).

6. Create a symbol for the full adder.

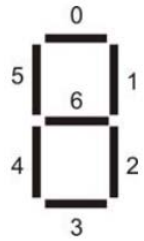
7. Create a symbol for the 4-bit adder.

8. Create a symbol for the seven segment display driver.

9. Create a new block diagram/schematic file to implement the up counter from PRE-LAB #2.

10. Compile, simulate and verify the designed 4-bit up counter.

11. Assign inputs and outputs. Use SW0 as a manual clock signal.

Inputs	**Switches**	**Outputs**	**HEX0**	
Clock	SW0	a	HEX0[0]	
Clear/Reset	SW1	b	HEX0[1]	
		c	HEX0[2]	
		d	HEX0[3]	
		e	HEX0[4]	
		f	HEX0[5]	
		g	HEX0[6]	

12. Demonstrate to your instructor.