

PRE-LAB

Design a sequential system that displays a sequence of number on a seven segment display (SSD) based on an input signal, x . Use D Flip Flops.

Requirements:

- When $x = 0$, the system sequences through 0, 1, 2, 3, 4, 0, 1, 2, ... (0 to 4 and repeat)
 - When $x = 1$, the system sequences through 2, 3, 4, 5, 6, 7, 2, 3, ... (2 to 7 and repeat)
 - If at any time, the system displays 5, 6, or 7 and $x = 0$, the next number should be displayed is 3.
 - If at any time, the system displays 0, or 1 and $x = 1$, the next number should be displayed is 3.
1. Draw a state diagram.
 2. Develop a state table.
 3. Derive the next state equations using K-Maps.
 4. Draw a circuit diagram. Include an active low *reset* signal to re-start the sequence at **number 3** if activated (*reset* = 0). Hint: use *CLR* and *PRE* options of the DFFs to reset your system to a specific state.

LAB

1. Create a new project (in a new directory/folder).
2. Create a new block diagram/schematic file to implement the designed circuit from PRELAB #4.
3. Compile, simulate, and verify the circuit.

The DE2 board provides a clock frequency of 50 MHz. However, in order to observe the operations of your circuit, you will need a much slower clock signal. A clock divider circuit to reduce the 50MHz clock to 1 Hz has been provided. This clock divider accepts the 50 MHz signal as an input (*clk_in*) and produces a 1 Hz signal (*clk_out*). A symbol of this clock divider is shown in Fig. 1.

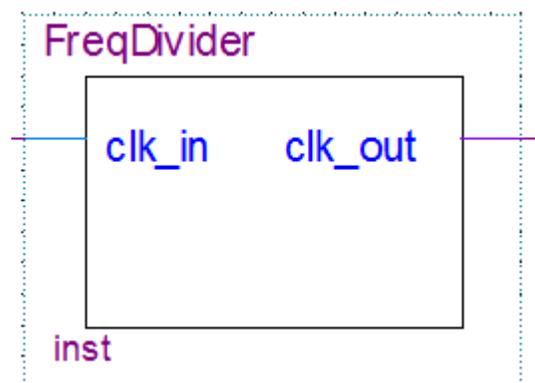
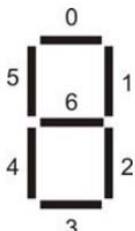


Fig. 1 Block diagram of a clock/frequency divider (50 MHz input, 1 Hz output).

Lab #7**EC262**

4. Download (Right click > Save As) the following 3 files from the syllabus page and add them to your project:
 - *freqDiv.vhd* (no modifications needed).
 - *FreqDivider.bdf* (no modifications needed).
 - *FreqDivider.bsf* (no modifications needed).
5. Add the clock divider symbol (*FreqDivider*) to your circuit and use the output *clk_out* of this symbol as the clock signal that is connected to all the flip flops. The input of this clock divider symbol should be connected to the 50 MHz clock signal on the DE2 board (see pin assignments below).
6. Assign Inputs/outputs

Inputs	Pins	Outputs	HEX0
Clock (50 MHz)	CLOCK_50	a	HEX0[0]
Clear/Reset	KEY[0]	b	HEX0[1]
X	SW0	c	HEX0[2]
		d	HEX0[3]
		e	HEX0[4]
		f	HEX0[5]
		g	HEX0[6]



7. Compile your design.
8. Program and demonstrate your design.