

**EC262 Problem Set 10**  
**Due: Wednesday 17 October 2012**

Complete the following problems from the textbook *Digital Design with an Introduction to the Verilog HDL*, Mano and Ciletti, Fifth Edition.

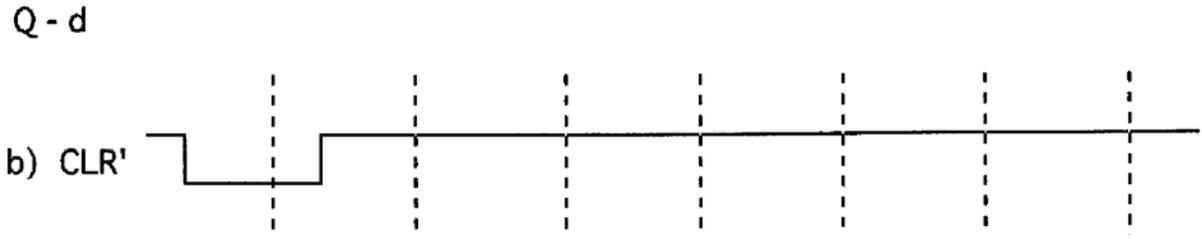
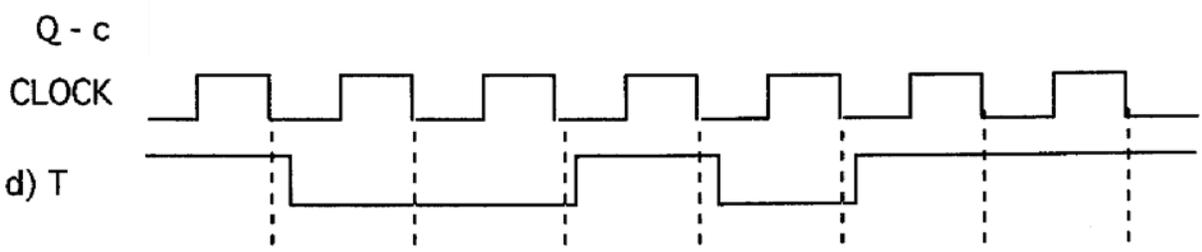
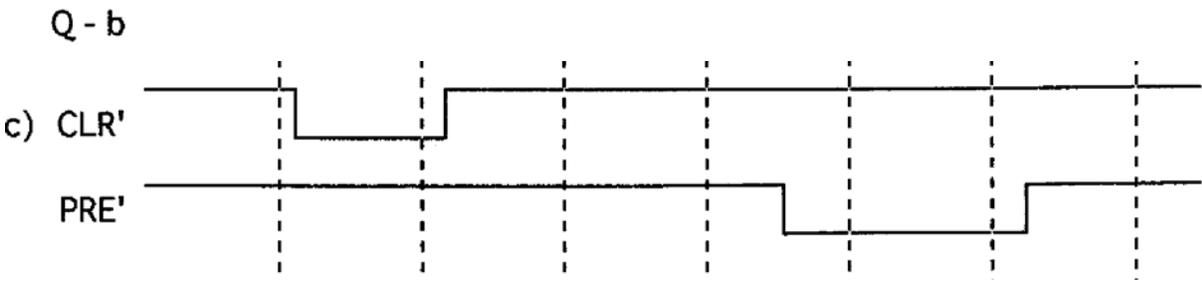
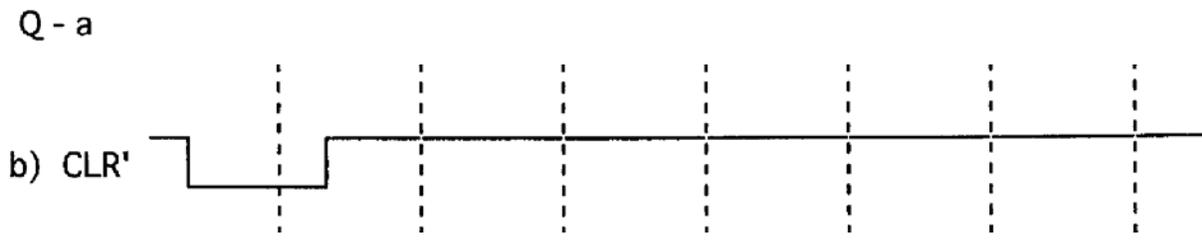
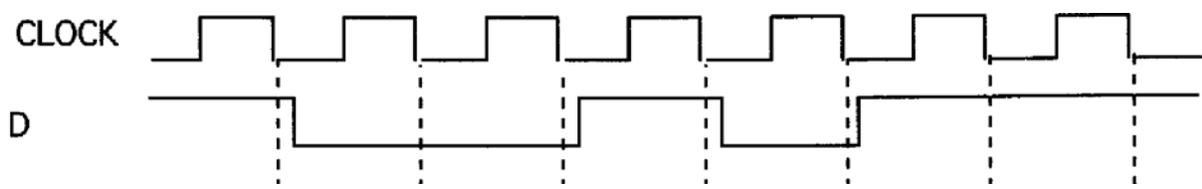
**Chapter 5**

Problems: 7, 8, 9

**Additional Problems**

**Exercise 1:** Complete the following timing diagram for a flip flop (FF)

- a. Assume that the FF is a DFF without a clear or preset
- b. Assume that the FF is a DFF with the same input as part a and an active low clear input.
- c. Assume that the FF is a DFF with the same input as part a and active low clear and preset inputs.
- d. Assume that the FF is a TFF without a clear or preset and that  $Q$  is initially 0.
- e. Assume that the FF is a TFF with the same input as part d and an active low clear input and that  $Q$  is initially 0.



**Exercise 2:** Complete the following timing diagram for a J-K flip flop. Assume that preset input is inactive.

