

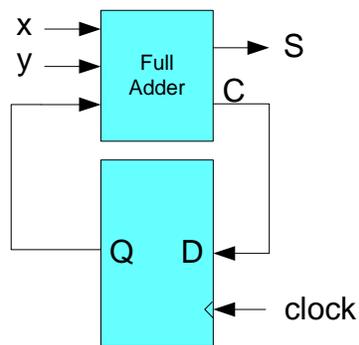
EC262 Problem Set 10
Due: Wednesday 17 October 2012

Complete the following problems from the textbook *Digital Design with an Introduction to the Verilog HDL*, Mano and Ciletti, Fifth Edition.

Chapter 5

Problems: 7, 8, 9

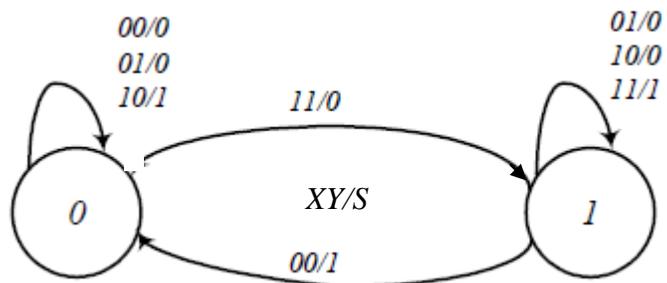
Problem 7:



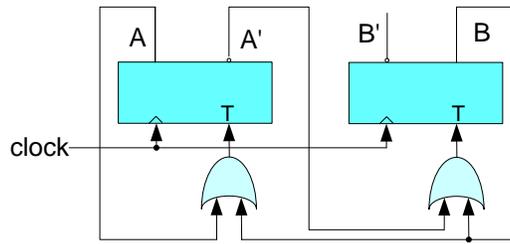
State table:

| Present state | Inputs | | Next state | Output |
|---------------|--------|---|------------|--------|
| Q | x | y | Q | S |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

State diagram:



Problem 8:



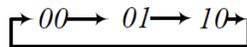
State table:

| Present state | | Next state | | FF Inputs | |
|---------------|---|------------|---|-----------|-------|
| A | B | A | B | T_A | T_B |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |

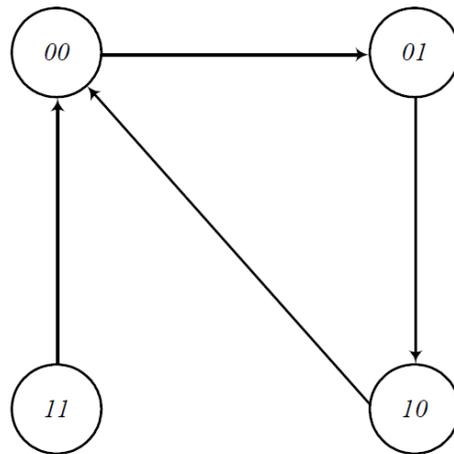
$$T_A = A + B$$

$$T_B = A' + B$$

Repeated sequence:



State diagram:



Problem 9: A sequential circuit has 2 JK flip flops A and B, one input x.

$$J_A = x \quad K_A = B$$

$$J_B = x \quad K_B = A'$$

- a. Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and K variables.

$$A^* = A(t+1) = J_A A' + K_A A = xA' + B'A$$

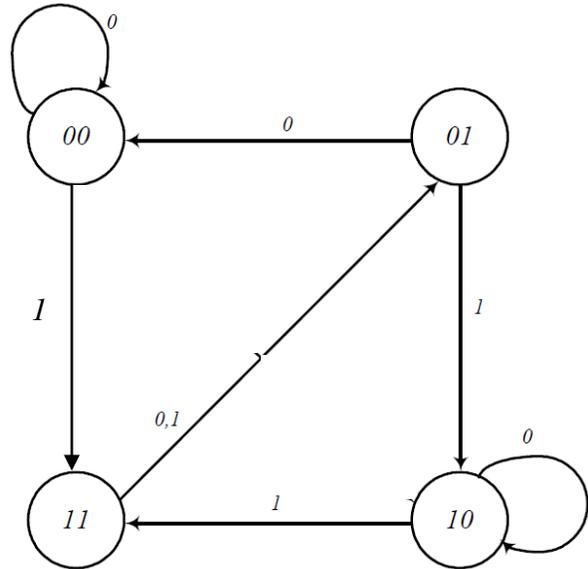
$$B^* = B(t+1) = J_B B' + K_B B = xB' + AB$$

b. State table and state diagram

State table:

| x | A B | | Next State | |
|-----|---------|-----|-------------|------------|
| | | | A^* | B^* |
| | A | B | $xA' + B'A$ | $xB' + AB$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |

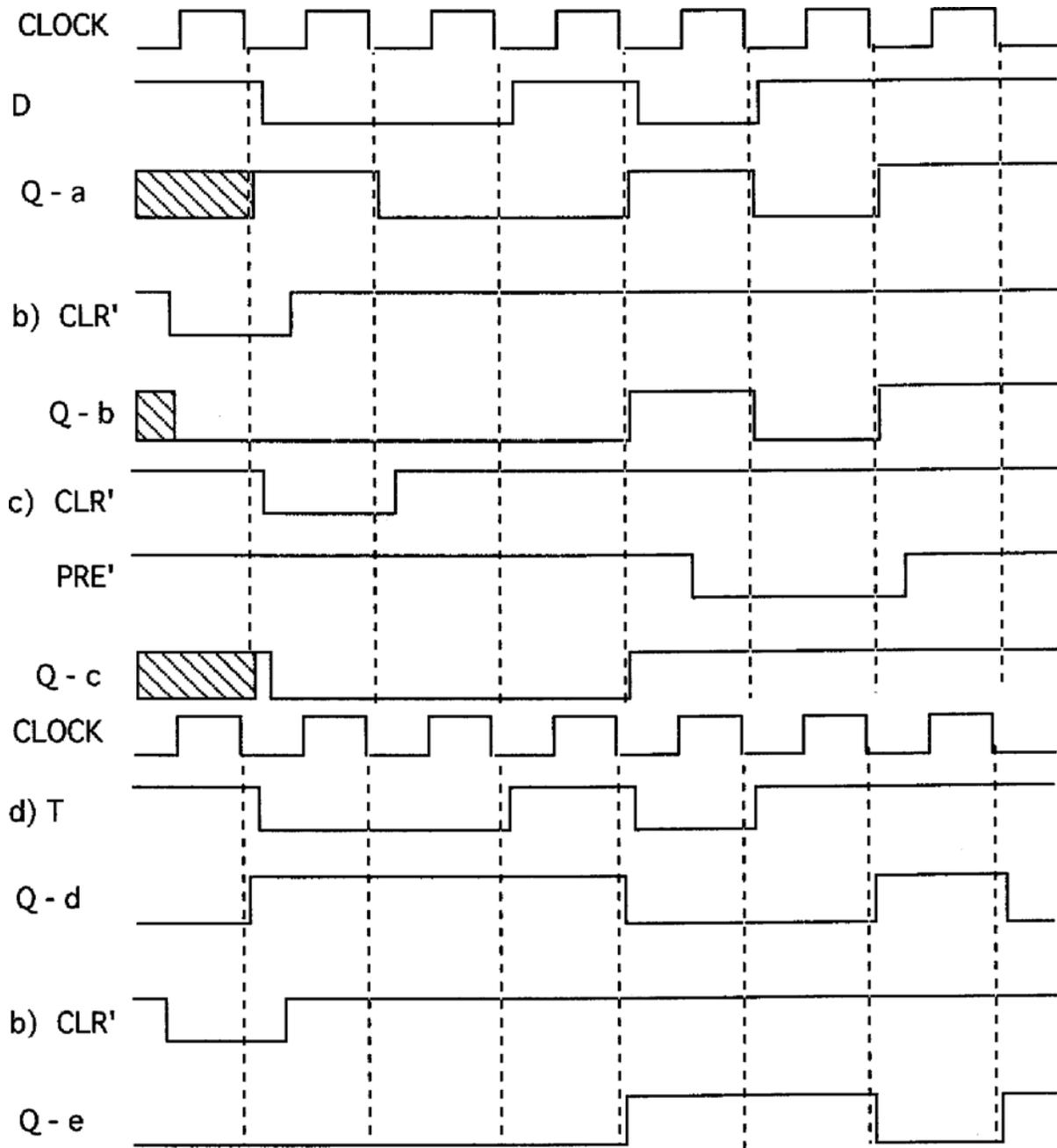
State diagram:



Additional Problems

Exercise 1: Complete the following timing diagram for a flip flop (FF)

- Assume that the FF is a DFF without a clear or preset
- Assume that the FF is a DFF with the same input as part a and an active low clear input.
- Assume that the FF is a DFF with the same input as part a and active low clear and preset inputs.
- Assume that the FF is a TFF without a clear or preset and that Q is initially 0.
- Assume that the FF is a TFF with the same input as part d and an active low clear input and that Q is initially 0.



Exercise 2: Complete the following timing diagram for a J-K flip flop. Assume that preset input is inactive.

