

EC262 Problem Set 11

Due: Monday 22 October 2012

Complete the following problems from the textbook *Digital Design with an Introduction to the Verilog HDL*, Mano and Ciletti, Fifth Edition.

Chapter 5

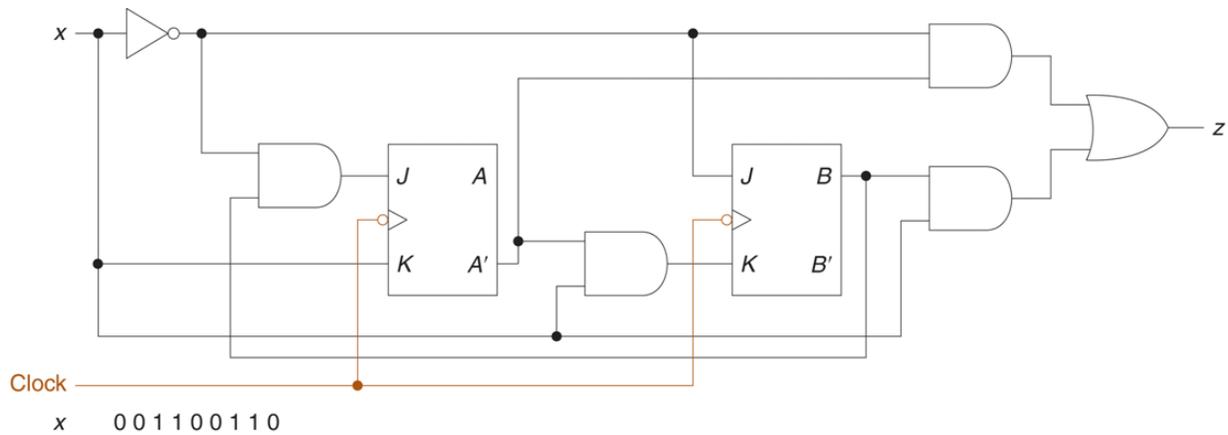
Problems: 10(b,c)

Additional Problems

Exercise 1: Construct a state diagram for the following state table

$q_1 q_2$	$q_1^* q_2^*$		z	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0 0	0 1	0 0	0	1
0 1	1 0	1 1	0	0
1 0	0 0	0 0	1	1
1 1	0 1	0 1	1	0

Exercise 2: For the given circuit



- a. Construct a state table
- b. Construct a state diagram.