

EC262 Problem Set 7 (Solutions)
Due: Wednesday 19 September 2012

Complete the following problems from the textbook *Digital Design with an Introduction to the Verilog HDL*, Mano and Ciletti, Fifth Edition.

Chapter 4

Problems: 14.

Additional Problems

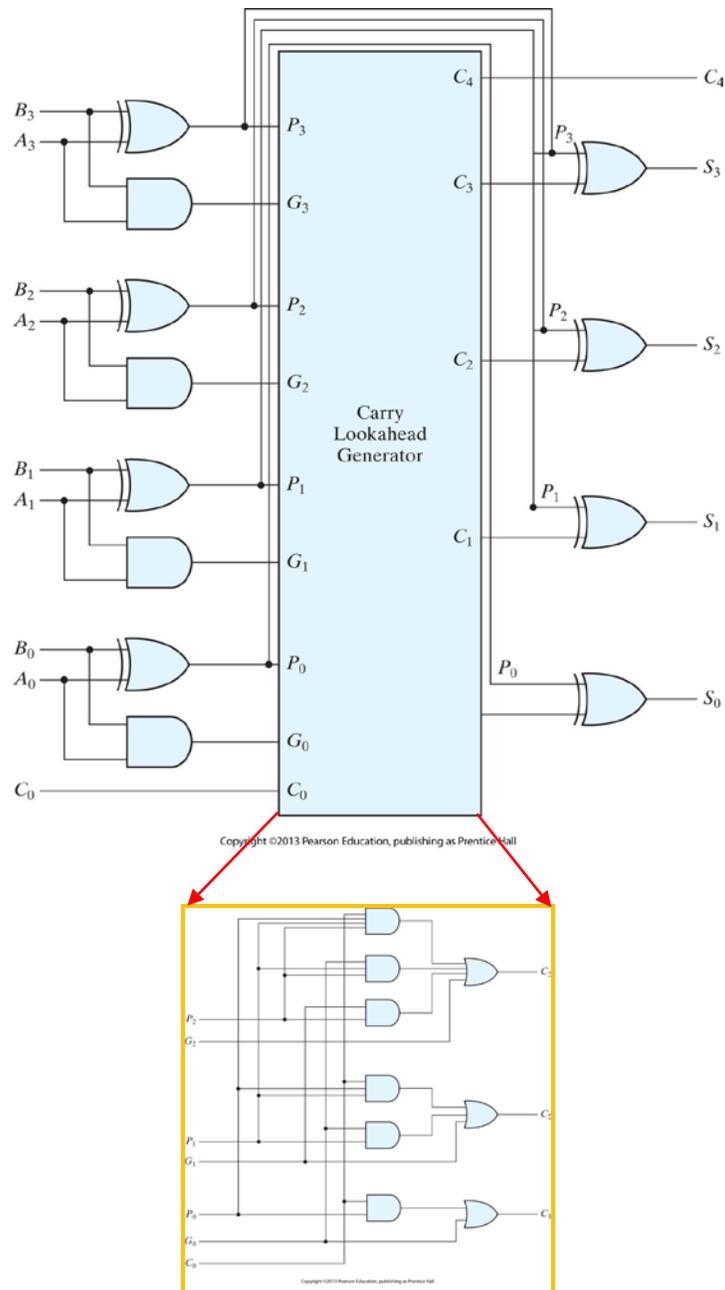
Exercise 1:

MIDN 3/C Worksalot wishes to design a “crab-ometer” to remind him when it is safe to eat Maryland blue crabs. From local acquaintances, he knows that crabs are safe to eat during months without an ‘r’ in their name (May, June, July and August) and in September and October. The eater might endure some unpleasant consequences if eaten during the remaining months of the year. The input to the "crab-ometer" function is the month encoded as a 4-bit digital number, $a_3a_2a_1a_0$ where January corresponds to 1_{10} and December corresponds to 12_{10} . The output should be on when it is safe to consume the crabs.

- a. Determine the minimum SOP expression for the output.
- b. Implement the function using NOT, AND and OR gates. Assume that only uncomplemented inputs are available.
- c. If the propagation delay of each gate is 10ns. Find the total (worst-case) propagation delay of the circuit in part b.

Chapter 4

14. Find the total propagation delay.



XOR = 10 ns AND + OR = 10ns XOR = 10ns

Total propagation delay = 10ns + 10ns + 10ns = 30ns

Additional Problems

Exercise 1:

a.

Month	Encoded binary number	Output
	$a_3a_2a_1a_0$	F
	0 0 0 0	X
Jan	0 0 0 1	0
Feb	0 0 1 0	0
Mar	0 0 1 1	0
Apr	0 1 0 0	0
May	0 1 0 1	1
Jun	0 1 1 0	1
Jul	0 1 1 1	1
Aug	1 0 0 0	1
Sep	1 0 0 1	1
Oct	1 0 1 0	1
Nov	1 0 1 1	0
Dec	1 1 0 0	0
	1 1 0 1	X
	1 1 1 0	X
	1 1 1 1	X

a_3a_2 a_1a_0	00	01	11	10
00	X			1
01		1	X	1
11		1	X	
10		1	X	1

$$F = a_2 a_0 + a_2 a_1 + a_3 a_2' a_1' + a_3 a_1 a_0'$$

or

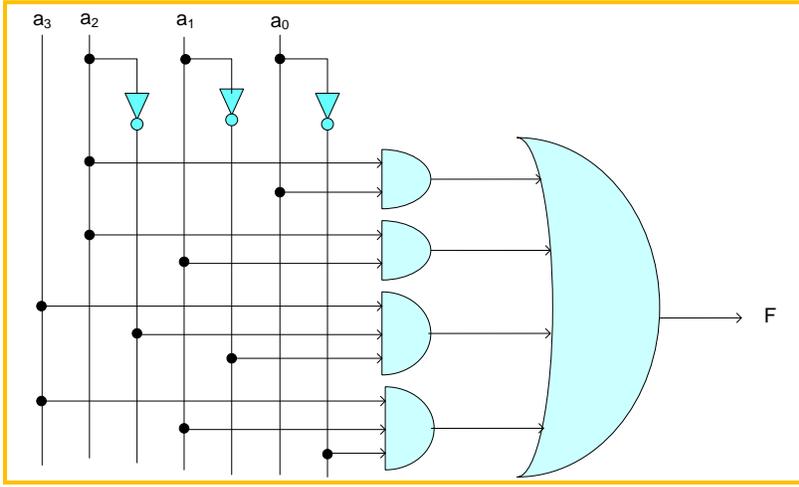
$$F = a_2 a_0 + a_2 a_1 + a_3 a_2' a_1' + a_3 a_2' a_0'$$

or

$$F = a_2 a_0 + a_2 a_1 + a_3 a_1' a_0 + a_3 a_2' a_0'$$

b.

$$F = a_2 a_0 + a_2 a_1 + a_3 a_2' a_1' + a_3 a_1 a_0'$$



c.

Total propagation delay = 30 ns