

EC262 Problem Set 8 (Solutions)
Due: Monday 24 September 2012

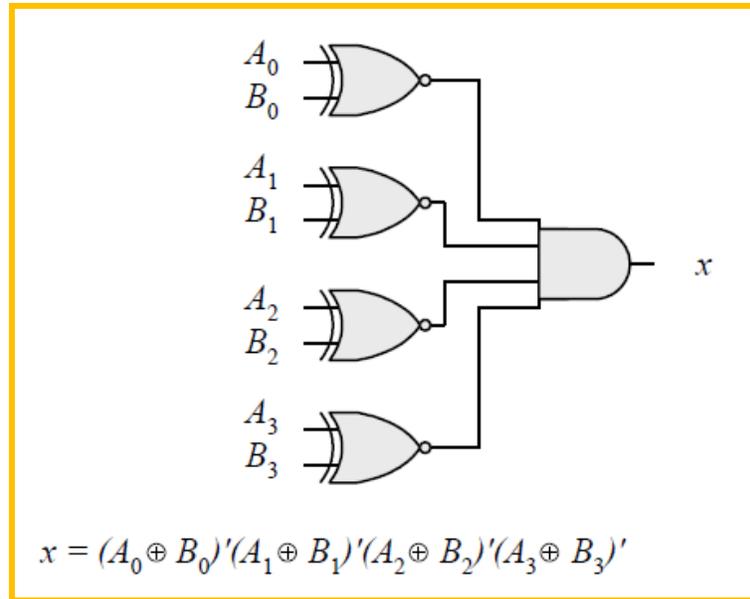
Complete the following problems from the textbook *Digital Design with an Introduction to the Verilog HDL*, Mano and Ciletti, Fifth Edition.

Chapter 4

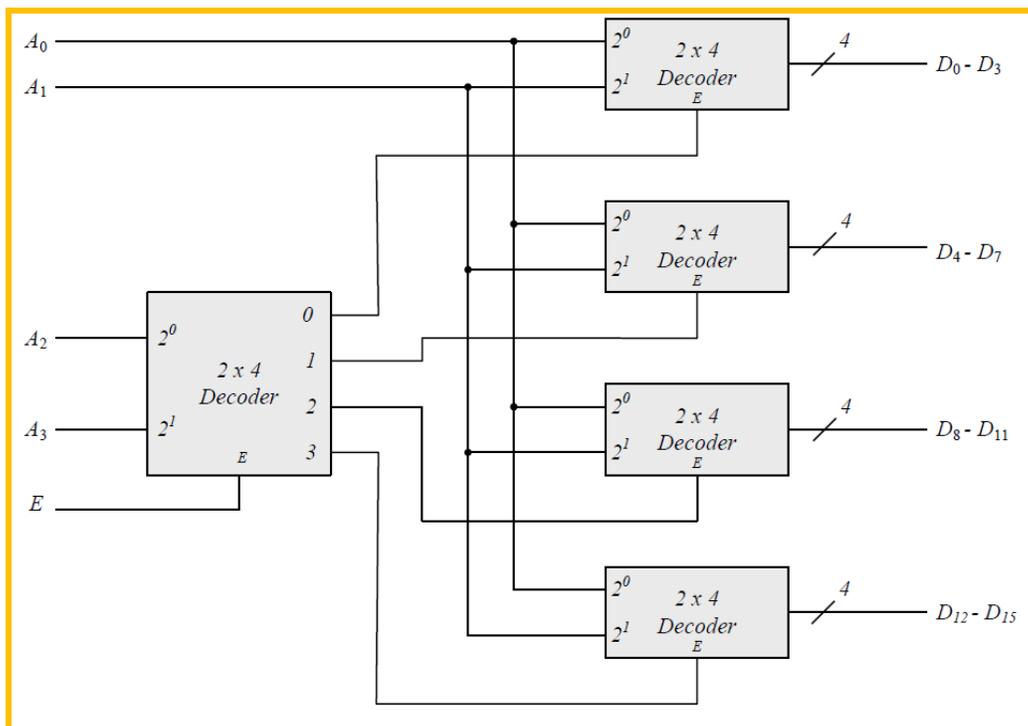
Problems: 21, 26, 28(a), 31, 32(a), 33.

Chapter 4

Problem 21: Design a combinational circuit that compares 2 4-bit numbers to check if they are equal.

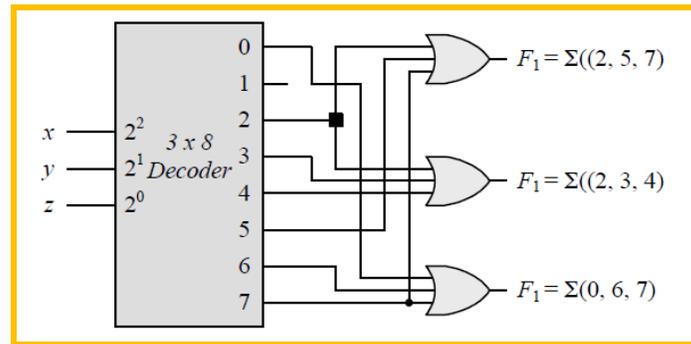


Problem 26: Construct a 4-to-16-line decoder with 5 2-to-4 decoders with enable.

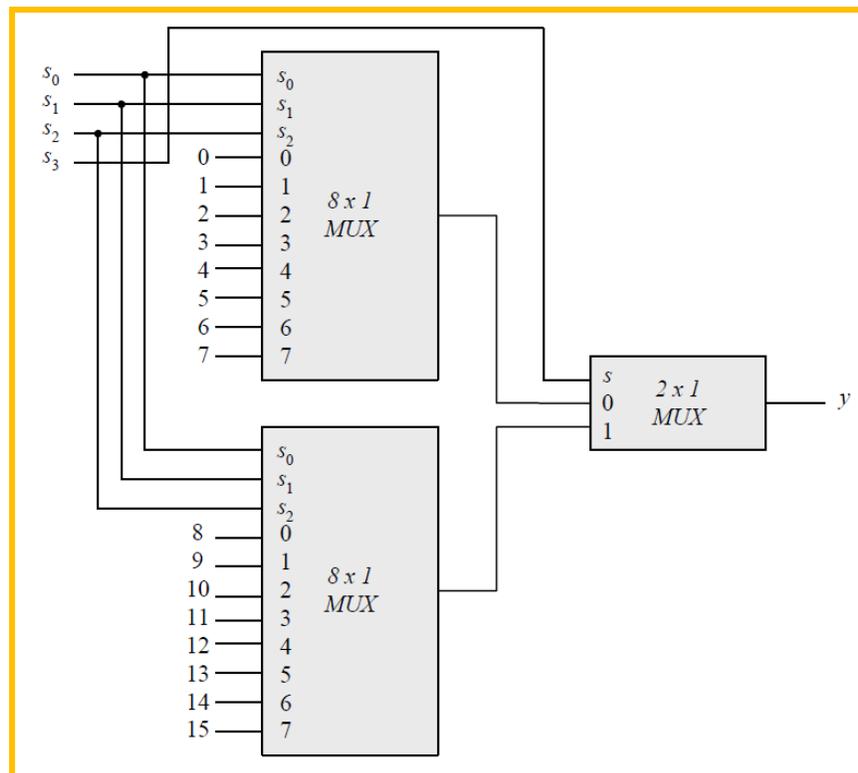


Problem 28: Using decoder and external gates, design the combinational circuits defined by the following functions.

- a. $F_1 = x'y'z' + xz = \Sigma(2, 5, 7)$
 $F_2 = xy'z' + x'z = \Sigma(2, 3, 4)$
 $F_3 = x'y'z' + xy = \Sigma(0, 6, 7)$



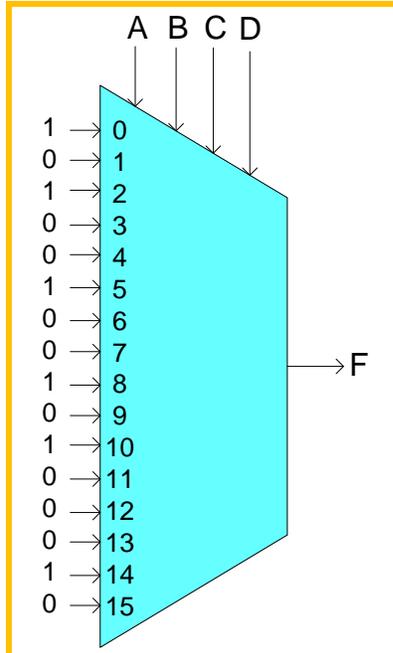
Problem 31: Construct a 16x1 multiplexer with 2 8x1 and 1 2x1 multiplexers.



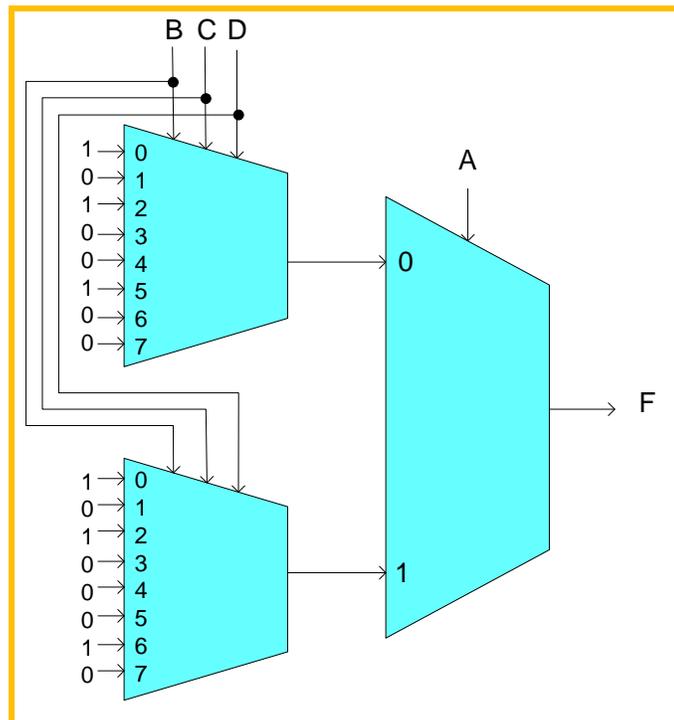
Problem 32: Implement the following function with a multiplexer.

a. $F(A,B,C,D) = \Sigma(0,2,5,8,10,14)$

Using one 16x1 multiplexer



Using two 8x1 and one 2x1 multiplexers



Problem 33: Implement a full adder with two 4x1 multiplexers.

Truth table for a FA:

ABC	Cout	Sum
000	0	0
001	0	1
010	0	1
011	1	0
100	0	1
101	1	0
110	1	0
111	1	1

Redraw table

AB	Cout		Cout	Sum		Sum
	C = 0	C = 1		C = 0	C = 1	
00	0	0	0	0	1	Ci
01	0	1	Ci	1	0	Ci'
10	0	1	Ci	1	0	Ci'
11	1	1	1	0	1	Ci

