1) (8 pts) True or False:

a. (True) False Silicon has four valence electrons.

b. (True) False An *n*-type semiconductor is created by doping with an element that contains one extra valence electron.

c. True (False) For a *pnp* BJT operating in the active region, both the emitter-base junction and the collector-base junction must be in forward bias.

d. True (False) When used as a switch, a BJT operates in the active and cutoff regions.

2) (10 pts) If silicon is doped with an acceptor concentration of $N_A = 10^{15}$ acceptor atoms/cm^3, determine the free electron concentration and the hole concentration.

$$p \approx N_A = \boxed{10^{15} \text{ holes/cm}^3}$$

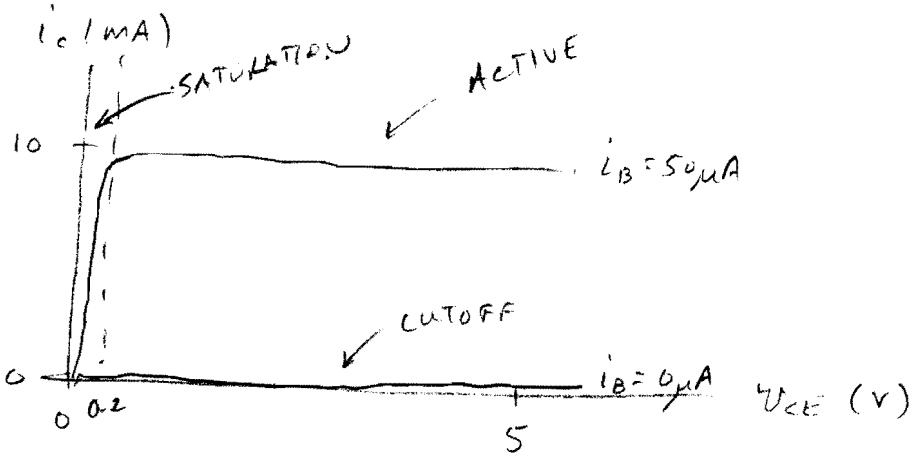
$$pn = n_i^2 = (1.45 \times 10^{10})^2$$

$$n = \frac{n_i^2}{p} = \frac{(1.45 \times 10^{10})^2}{10^{15}} = \boxed{2.1 \times 10^5 \text{ ELECTRONS/cm}^3}$$

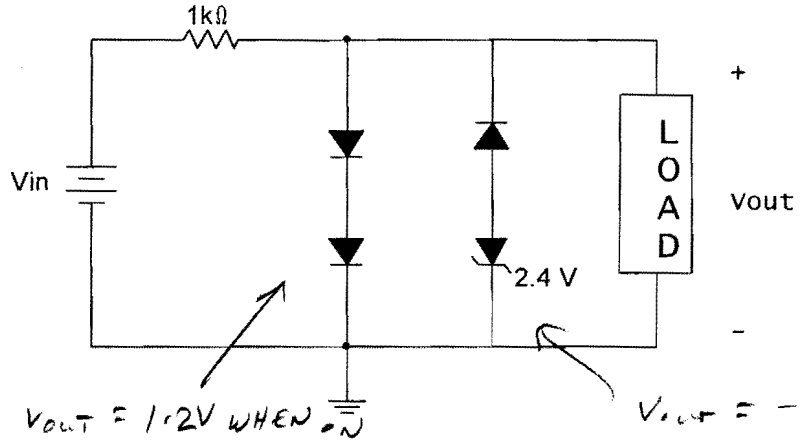
3) (4 pts) Drift current results due to the motion of electrons in the presence of an electric field. Diffusion current results due to a concentration gradient at a *p-n* junction. (Fill in the blanks.)

4) (13 pts) In the space below, sketch the output characteristic (i_C vs. v_{CE}) for an *npn* BJT with $\beta = 200$ over the v_{CE} range of 0 to 5 V. Show lines for $i_B = 0$ and 50 μA. Label and scale the axes. Identify the cutoff, active and saturation regions on the plot.

$i_c = \beta i_B = 200(50\mu) = 10\text{mA}$

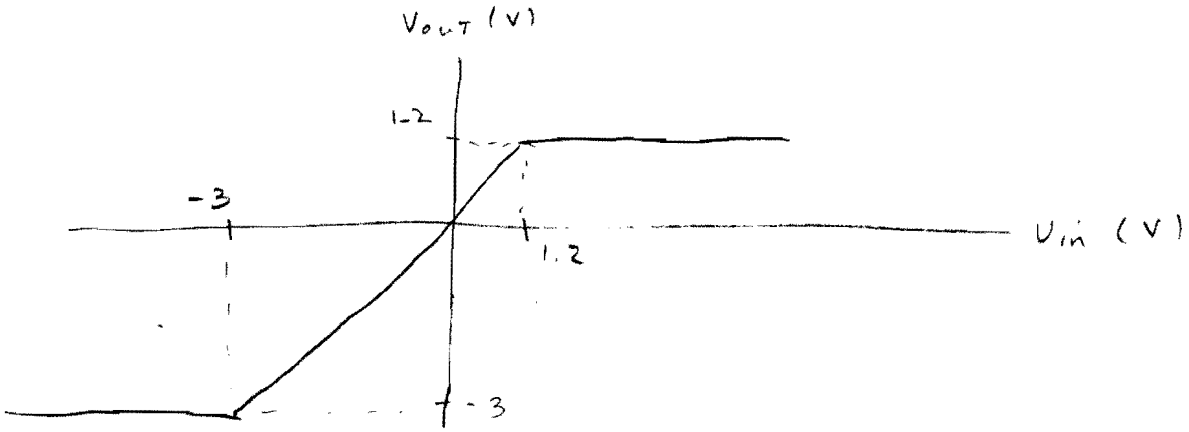


5) (25 pts) In the circuit below, each diode drops 0.6 V in forward bias.



VOUT = VIN IF DIODES OFF

a. (10 pts) Assume a no load condition and plot v_{out} as a function of v_{in} for -6 V < v_{in} < 6 V. Label axes clearly and include units.



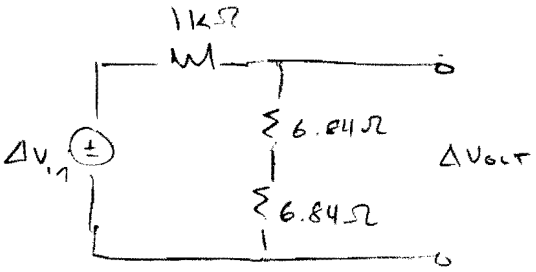
b. (15 pts) For the no load condition, compute the source regulation when v_{in} = 5V. (Hint: Assume that n = 1 and use a small-signal model for the diodes.)

TWO DIODES ON IN LEFT BRANCH

VOUT = 1.2 V

$$I_{DQ} = \frac{5 - 1.2}{1k} = 3.8\,mA$$

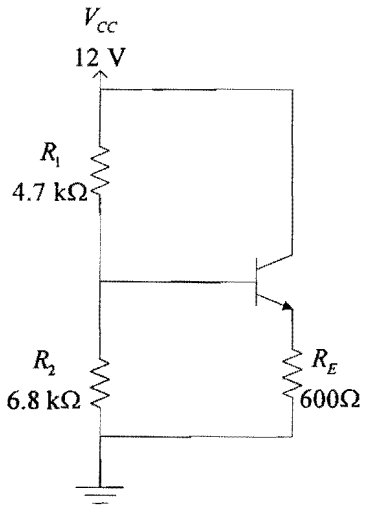
$$r_d = \frac{nV_T}{I_{DQ}} = \frac{26m}{3.8m} = 6.84\,\Omega$$



$$SR = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\% = \frac{2(6.84)}{1k + 2(6.84)} \times 100\%$$

$$= \boxed{1.35\%}$$

6) (20 pts) The bias circuit shown below is used to set the Q-point of an Emitter-Follower amplifier.



To prevent distortion in the amplifier output signal, the circuit was designed to maintain a collector-emitter voltage of 5.7 V < V_{CEQ} < 6.3 V. Solve for the minimum value of β for the BJT. Assume that V_{BEQ} = 0.7V.

THEVENIZE

$$V_B = 12 \frac{6.8}{6.8+4.7} = 7.10\,V$$

$$R_B = 4.7 \| 6.8 = 2.78\,k\Omega$$

$$V_B - V_{BE} = I_B R_B + I_E R_E = \frac{I_E}{\beta+1} R_B + I_E R_E$$

$$I_E = \frac{V_B - V_{BE}}{\frac{R_B}{\beta+1} + R_E}$$

FOR β_{min}, I_E SMALLER $\Rightarrow$ β_{min} OCCURS AT MAX V_{CE}, OR $V_{CE} = 6.3\,V$

$V_{CE} = 6.3\,V$

$$V_E = 5.7\,V \Rightarrow I_E = \frac{5.7}{600} = 9.5\,mA = \frac{7.1 - 0.7}{\frac{2.78k}{\beta+1} + 600}$$

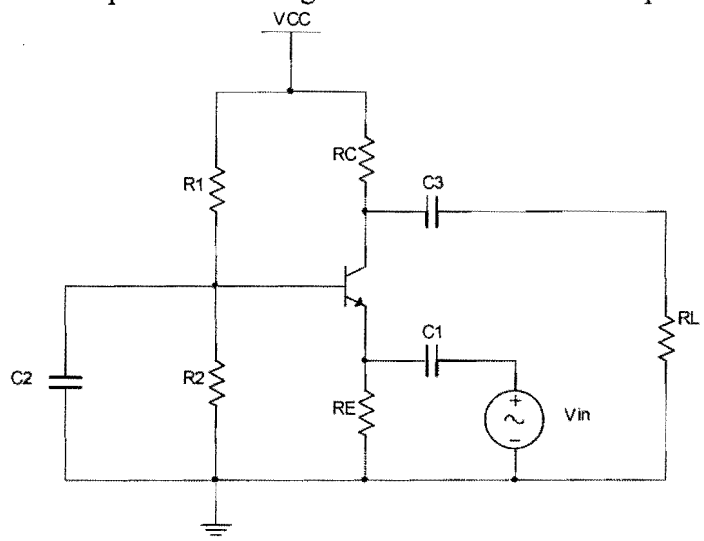
$$\frac{2.78k}{\beta+1} + 600 = \frac{6.4}{9.5m}$$

$$\frac{2.78k}{\beta+1} = \frac{6.4}{9.5m} - 600 \Rightarrow \beta + 1 = 37.7$$

$$\beta = 36.7$$

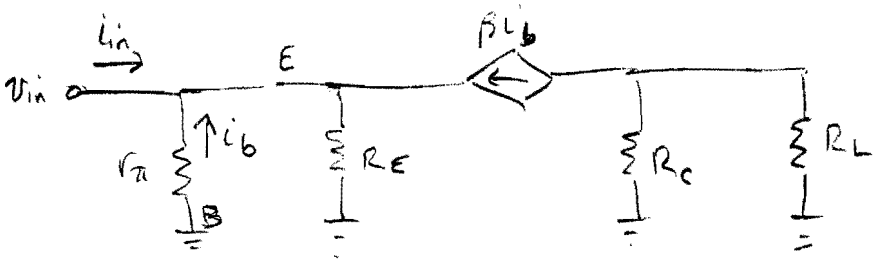
β_{min} = 36.7

7) (20 pts) Assume that all the capacitors are large in the common base amplifier shown below.



a. (10 pts) Draw the small-signal model for the circuit in terms of r_π, β and the resistor values. (Hint: Carefully consider which **resistors** are shorted out by the capacitors!)

R_1, R_2 SHORTED BY C_2 $\Rightarrow$ BASE @ GND, INPUT AT EMITTER



b. (10 pts) Determine an expression for the **input impedance Z_{in}** seen by the AC source. Write the expression in terms of r_π, β and the resistor values.

$$i_{in} = \frac{v_{in}}{r_\pi} + \frac{v_{in}}{R_E} - \beta i_b \qquad \text{WHERE } i_b = -\frac{v_{in}}{r_\pi}$$

$$= \frac{v_{in}}{r_\pi} + \frac{v_{in}}{R_E} + \frac{\beta v_{in}}{r_\pi} = v_{in}\left(\frac{1}{R_E} + \frac{\beta+1}{r_\pi}\right)$$

$$Z_{in} = \frac{v_{in}}{i_{in}} = \underline{R_E \parallel \frac{r_\pi}{\beta+1}}$$