

**Short answer questions:**

1. (4 pts) Circle true or false for each statement below:

True    False CMOS is used for complex digital integrated circuit design because the static power dissipation of a CMOS logic gate is minimal.

True    False An increase in the fanout may not impact the power dissipation if there is a corresponding decrease in the switching frequency of the logic gates.

2. (6 pts) Fill in the blanks. When biased above threshold, the channel of a MOSFET behaves like a (short) resistor if the voltage between the drain and the source is relatively small. In this switch case, the FET is biased in the triode region.

3. (4 pts) Identify the relationships between  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ , and  $V_{IL}$  that are required to insure that the noise margins  $NM_H$  and  $NM_L$  are positive,

$$V_{OH} > V_{IH} \quad V_{OL} < V_{IL}$$

4. (6 pts) Given  $V_{GS} = 4V$ ,  $V_{to} = 2V$ ,  $K_P = 50 \mu A/V^2$ ,  $L = 10 \mu m$  and  $W = 400 \mu m$ , determine the value of  $V_{DS}$  where the FET transitions between the triode and saturation regions.

$$\text{AT TRANSITION } V_{GS} - V_{to} = V_{DS}$$

$$V_{DS} = 4 - 2 = \boxed{2V}$$

5. (10 pts) Given a source voltage of 5 V, a drain resistance of  $1 k\Omega$ , and a switching frequency of 10 MHz, determine the gate capacitance required to support rise times less than 10 ns and dynamic power consumption less than 1 mW per logic gate.

$$\text{For } P_{dyn} \leq 1 \text{ mW} \quad f C V_{DD}^2 = 10M(s)(s^2) \leq 1 \text{ mW}$$

$$C \leq \frac{1 \text{ mW}}{10M(s)^2} = 4 \text{ pF}$$

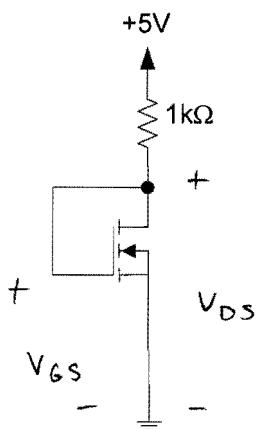
FOR  $t_{PLH} \leq 10 \text{ ns}$

~~0.69312~~ ~~C~~ ~~E~~ ~~10ns~~  
Wrong eqn here - need eqn for  
 $t_r = 2.202 \cdot C$  —  $C$  still  $\leq 4 \text{ pF}$

$$1k\Omega \quad C \leq \frac{10n}{0.6931(1k\Omega)} = 14.4 \text{ pF}$$

**Problems:**

1. (25 pts) Assume the threshold voltage is  $V_{to} = 1$  V for the MOSFET in the circuit below, and that the device parameter  $K = 0.5 \text{ mA/V}^2$ . Assume the transistor is in saturation, and use the appropriate transistor equation and the load-line equation to find the drain current  $I_{DQ}$  and drain-source voltage  $V_{DSQ}$  at the operating point  $Q$ .



$$V_{GS} = V_{DS} \quad \text{so} \quad V_{DS} > V_{GS} - V_{to}$$

SATURATION ✓

$$V_{to} = 1\text{V}$$

$$K = 0.5 \text{ mA/V}^2$$

$$\begin{aligned} i_D &= \frac{5 - V_{DS}}{1k} = K(V_{DS} - V_{to})^2 \\ &= 0.5m(V_{DS} - 1)^2 \end{aligned}$$

$$5 - V_{DS} = 0.5(V_{DS} - 1)^2$$

$$10 - 2\sqrt{V_{DS}} = V_{DS}^2 - 2\sqrt{V_{DS}} + 1$$

$$9 = V_{DS}^2 \quad V_{DSQ} = \boxed{3\text{V}}$$

$$I_{DSQ} = \frac{5 - V_{DS}}{1k} = \frac{2}{1k} = \boxed{2\text{mA}}$$

2. (25 pts) Design a resistor pull-up NMOS inverter that meets the following specifications:

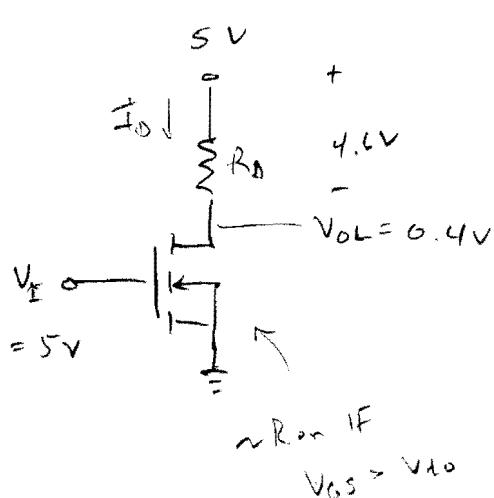
$$V_{OL} = 0.4 \text{ V}$$

$$V_{OH} = V_{DD} = 5 \text{ V}$$

$$K = 12 \mu\text{A/V}^2$$

$$P_{\text{static}} = 0.2 \text{ mW}$$

Determine both the value of the pull-up resistor that is needed, as well as the threshold voltage required in the MOSFET. Draw the final circuit.



$$P_{\text{static}} = V_{DD} I_D$$

$$I_D = \frac{P_{\text{static}}}{V_{DD}} = \frac{0.2 \text{ m}}{5} = 40 \mu\text{A}$$

$$R_D = \frac{4.6 \text{ V}}{40 \mu\text{A}} = \boxed{115 \text{ k}\Omega}$$

$$R_{on} = \frac{0.4 \text{ V}}{40 \mu\text{A}} = 10 \text{ k}\Omega = \frac{1}{2K(V_I - V_{t0})}$$

$$V_I - V_{t0} = 5 - V_{t0} = \frac{1}{2(12 \mu\text{A}) 10 \text{ k}}$$

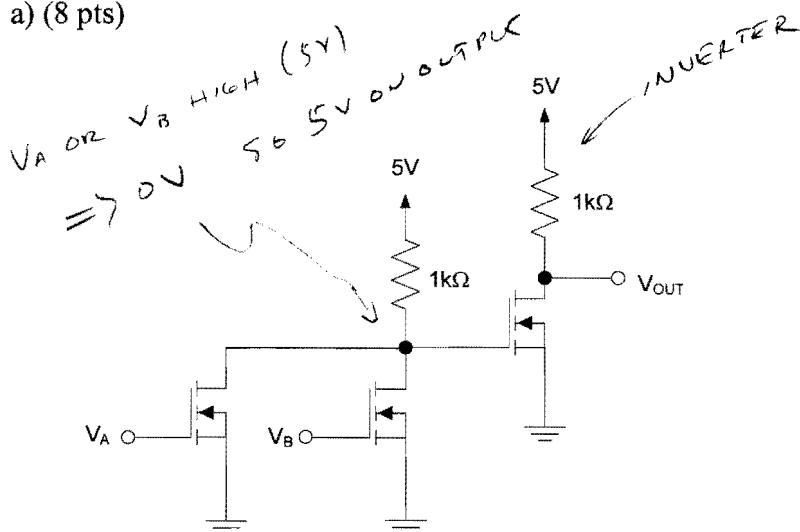
$$= 4.167 \text{ V}$$

$$V_{t0} = 5 - 4.167$$

$$= \boxed{0.833 \text{ V}}$$

3. (20 pts) Consider the two logic circuits shown below. Fill in the output voltages in each truth table and determine the logic function implemented by each circuit.

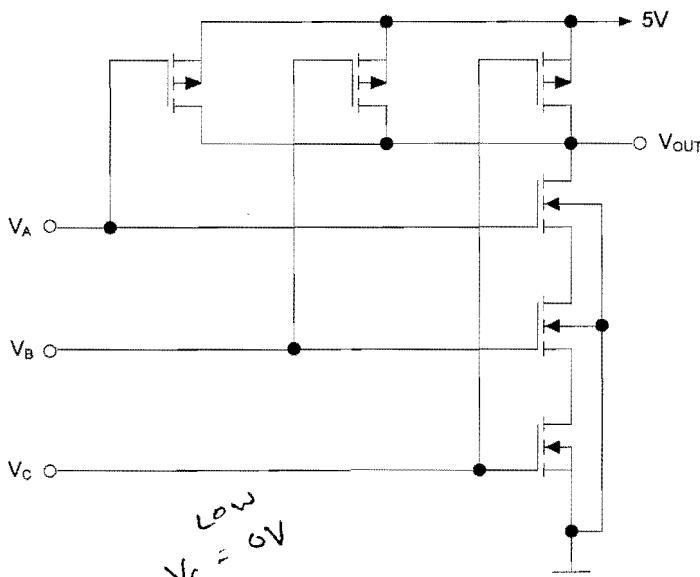
a) (8 pts)



| V <sub>A</sub> | V <sub>B</sub> | V <sub>OUT(V)</sub> |
|----------------|----------------|---------------------|
| 0V             | 0V             | 0 V                 |
| 0V             | 5V             | 5 V                 |
| 5V             | 0V             | 5 V                 |
| 5V             | 5V             | 5 V                 |

$$\text{OUT} = f(A, B) = \underline{\underline{A + B}}$$

b) (12 pts)



| V <sub>A</sub> | V <sub>B</sub> | V <sub>C</sub> | V <sub>OUT(V)</sub> |
|----------------|----------------|----------------|---------------------|
| 0V             | 0V             | 0V             | 5V                  |
| 0V             | 0V             | 5V             | 5V                  |
| 0V             | 5V             | 0V             | 5V                  |
| 0V             | 5V             | 5V             | 5V                  |
| 5V             | 0V             | 0V             | 5V                  |
| 5V             | 0V             | 5V             | 5V                  |
| 5V             | 5V             | 0V             | 5V                  |
| 5V             | 5V             | 5V             | 0V                  |

$$\text{OUT} = f(A, B, C) = \underline{\quad ABC \quad}$$

**SOME EQUATIONS**

$$K = \left( \frac{W}{L} \right) \frac{KP}{2}$$

$$KP = \mu_n C_{ox}$$

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2], \quad 0 \leq v_{DS} \leq v_{GS} - V_{to}$$

$$i_D = K(v_{GS} - V_{to})^2, \quad v_{DS} \geq v_{GS} - V_{to}$$

$$P_{dynamic} = f CV_{DD}^2$$

$$R_{on} = \frac{1}{2K(v_{GS} - V_{to})}$$

$$t_{PLH} = 0.6931 R_D C$$