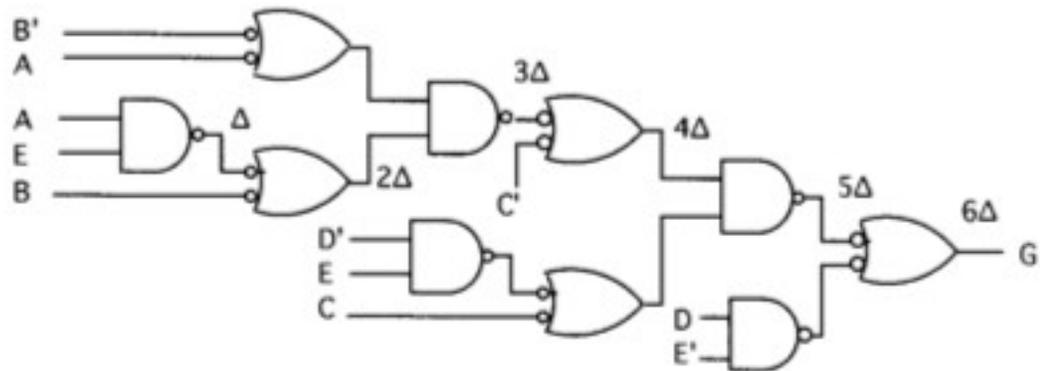


Homework 11 Solutions

1.

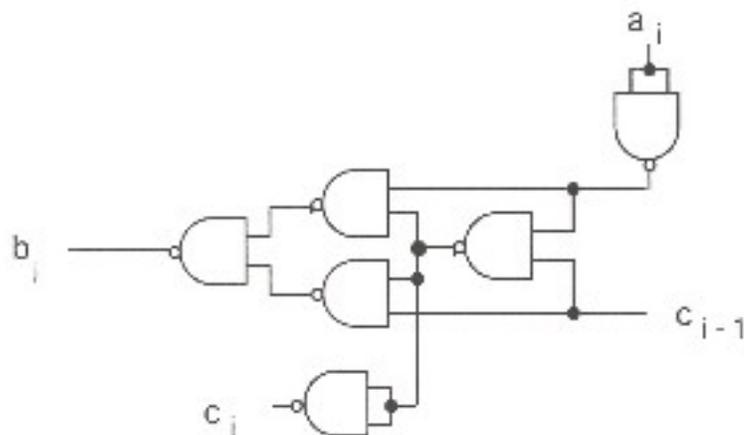


- 6Δ
- Also 6Δ , since B' passes through only 5 gates.
- 3Δ

- $$b_i = a_i c_{i-1} + a_i' c_{i-1}' = (a_i \oplus c_{i-1})' = a_i' \oplus c_{i-1}$$

$$c_i = a_i' c_{i-1}$$

For the least significant bit, the c input is 1, and thus, $b_0 = a_0$ and $c_0 = a_0'$. The circuit for the typical bit (using NAND gates) is



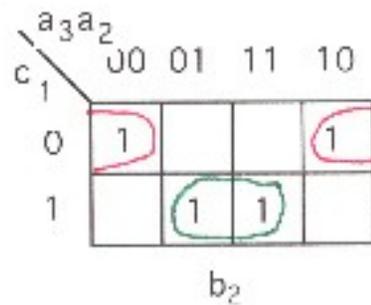
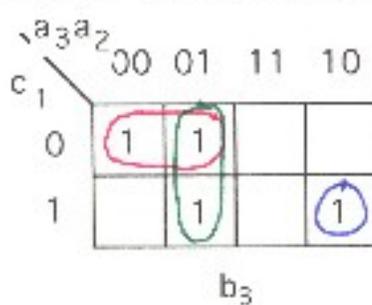
- The delay is $2n + 1$.
- The truth table for the second module is

Homework 11 Solutions

a_3	a_2	c_1	c_3	b_3	b_2
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	0	0	1
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	0	1

$$c_3 = a_3' a_2' c_1$$

The maps for the other outputs are:



$$b_3 = \underline{a_3' c_1'} + \underline{a_3' a_2} + \underline{a_3 a_2' c_1}$$

$$b_2 = \underline{a_2' c_1'} + \underline{a_2 c_1}$$

The circuit for b_3 is the same as that for b_1 in part a. That for c_3 requires a three input NAND and a NOT, producing a delay of 2 for each 2-bit stage. The circuit for b_3 requires four NANDS.

The total delay is $n + 1$ (two delays per two bits).