

Homework 17 Solutions

2.1

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY mux IS
    PORT (a, b : IN std_logic_vector( 7 downto 0);
          sel : IN std_logic_vector(1 downto 0);
          c   : OUT std_logic_vector(7 downto 0));
END mux;

ARCHITECTURE example OF mux IS
BEGIN
    PROCESS( a, b, sel )
    BEGIN
        IF (sel = "00") THEN
            c <= "00000000";
        ELSIF (sel = "01") THEN
            c <= a;
        ELSIF (sel = "10") THEN
            c <= b;
        ELSE
            c <= (OTHERS => '0');
        END IF;
    END PROCESS;
END example;
```

2.2 a

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY nand_func IS
    PORT (a, b, c : IN std_logic;
          d   : OUT std_logic);
END nand_func;

ARCHITECTURE d_out OF nand_func IS
BEGIN
    d <= NOT( a AND ( ( a AND b) OR NOT c));
END d_out;
```

Alternate solution

```
d <= a NAND ( ( a AND b) OR NOT c);
```

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