

Homework 20 Solutions

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LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY parity_chk IS
PORT (clk : IN std_logic;
      data : IN std_logic_vector(7 downto 0);
      parity : OUT std_logic);
END parity_chk;

ARCHITECTURE behavior OF parity_chk IS
BEGIN
PROCESS (clk)
    VARIABLE temp1: INTEGER RANGE 0 TO 8;
    VARIABLE temp2: INTEGER RANGE 0 TO 8;
BEGIN

    IF (clk'EVENT and clk = '1') THEN
        temp1 := 0;
        temp2 := 0;
        WHILE (temp2 <= 7) LOOP
            IF (data(temp2) = '1') THEN
                temp1 := temp1 + 1;
            END IF;
            temp2 := temp2 + 1;
        END LOOP;

        CASE temp1 IS
            WHEN 0 => parity <= '0';
            WHEN 1 => parity <= '1';
            WHEN 2 => parity <= '0';
            WHEN 3 => parity <= '1';
            WHEN 4 => parity <= '0';
            WHEN 5 => parity <= '1';
            WHEN 6 => parity <= '0';
            WHEN 7 => parity <= '1';
            WHEN 8 => parity <= '0';
            WHEN OTHERS => NULL;
        END CASE;
    END IF;
END PROCESS;
END behavior;
```