

Homework 21

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LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY state IS
    PORT (rst, inp, clk : IN std_logic;
          outp : OUT std_logic_vector(1 DOWNTO 0));
END state;

ARCHITECTURE behavior OF state IS
    TYPE state IS (S1, S2, S3, S4);
    SIGNAL pr_state, nx_state : state;
BEGIN
    PROCESS (rst, clk) BEGIN
        IF (rst = '1') THEN
            pr_state <= S1;
        ELSIF (clk'EVENT AND clk = '1') THEN
            pr_state <= nx_state;
        END IF;
    END PROCESS;
    PROCESS (inp, pr_state) BEGIN
        CASE pr_state IS
            WHEN S1 =>
                outp <= "00";
                IF (inp = '1') THEN
                    nx_state <= S2;
                ELSE nx_state <= S1;
                END IF;
            WHEN S2 =>
                outp <= "01";
                IF (inp = '1') THEN
                    nx_state <= S4;
                ELSE nx_state <= S3;
                END IF;
            WHEN S3 =>
                outp <= "10";
                IF (inp = '1') THEN
                    nx_state <= S4;
                ELSE nx_state <= S3;
                END IF;
            WHEN S4 =>
                outp <= "11";
                IF (inp = '1') THEN
                    nx_state <= S1;
                ELSE nx_state <= S2;
                END IF;
        END CASE;
    END PROCESS;
END behavior;
```