

PRE-LAB

Using either VHDL, schematic file (flip-flops and logic gates), or a combination of both design and simulate a state machine that implements a scrolling ALPHA code display on the dual seven-segment Altera board. Your state machine should follow the example below which uses an alpha code of 081234:

| LEFT digit | RIGHT digit |
|------------|-------------|
| blank | blank |
| blank | 0 |
| 0 | 8 |
| 8 | 1 |
| 1 | 2 |
| 2 | 3 |
| 3 | 4 |
| 4 | blank |

REPEAT

The state machine should scroll at a frequency of 1 Hertz.

Suggestions: This might be a good time take advantage of an 8-element 1-D ARRAY of 7-bit STD_LOGIC_VECTORS to hold the contents to be displayed on the SSDs. This is not necessary, but might make the code easier.

LAB

Implement your design on the Altera board and demonstrate its functionality to your instructor.