

LAB 5

PRE-LAB

Use the SR FF design provided in the supplement or the one provided in the textbook on page 369. Simulate and verify the behavior against the state table derived in class for the SR. Note for simulation, do not group CLK with the other inputs. Also, have CLK count separately and at a faster period than the other inputs. To do this: 1) Highlight your CLK, 2) Select the “Count” tab, 3) Select the Timing tab, and 4) Change it to count every 1.8 ns instead of 10 ns.

Afterwards, make a symbol out of this so that you can use it in the next two FF designs. In a new project, implement a D FF based on the SR (according to the supplement). Simulate and get state table and diagram from the simulation.

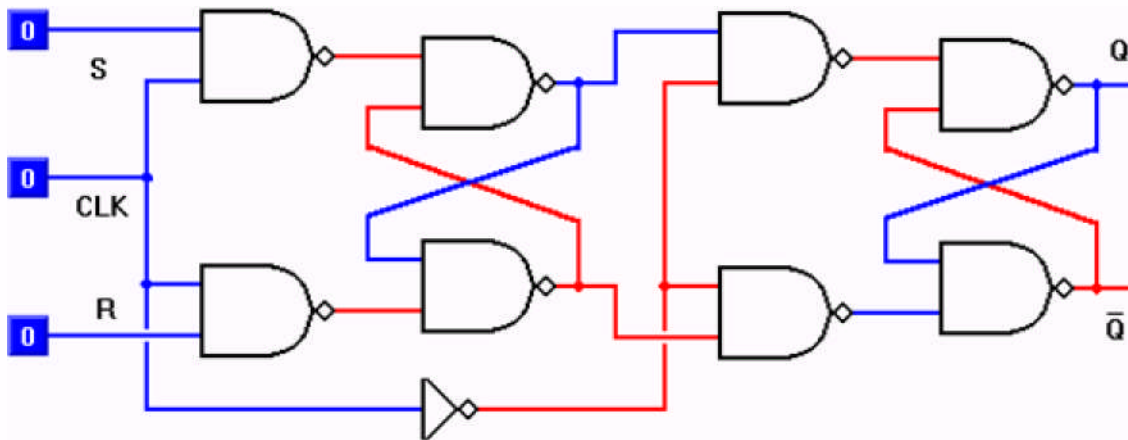
Then use a D FF from the quartus library and compare to the D FF you made.

Implement a JK and T FF based on the SR FF.

LAB

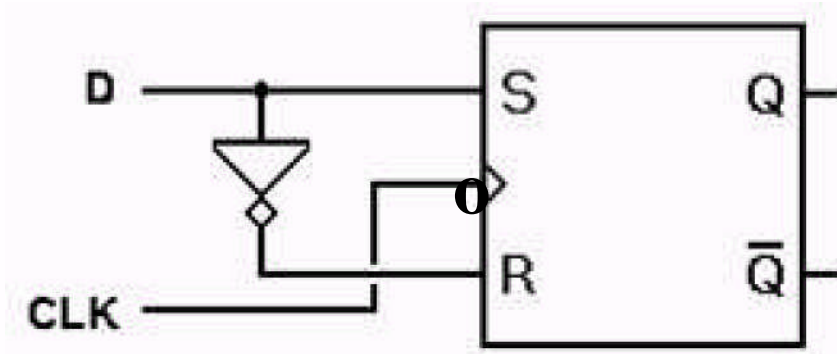
Implement your designs on the Altera board and demonstrate functionality to your instructor.

SR FF (Could use NOR or NAND)



You could use this one or the NOR implementation from the textbook

Make a D from an SR



Make a JK from a D

