

PRE-LAB

Using D or JK flip-flops in schematic style, design and simulate a synchronous counter that counts from 0 – 9 and repeats. Include in your design an output function that has a logic value of 1 while the counter has a value of 9 and is otherwise a logic value of 0. Also include an asynchronous reset that takes you back to 0 (use the preset/clear of the FFs in storage to accomplish this).

LAB

Using a manual clock as your input, implement your design on the Altera board and demonstrate its functionality to your instructor.