

EE 242 Lab #8

PRE-LAB

Using VHDL, design and simulate a Moore state machine that implements the state diagram from problem 8.1 of your Pedroni book. You should have a reset that resets the machine to state 1.

LAB

Implement your design on the Altera board. Please use a manual clock and hex numbers to demonstrate your work. Hint: are the seven segment displays active low or high?