

**PRE-LAB**

Using VHDL, design and simulate a Moore state machine that implements the state table shown below. Note that there are two INPUT bits (00, 01, 10, and 11 in the table) and that the state machine should output logic high when states C, E or G occur. Please use a 3-5 second clock to demonstrate. You should have a reset that resets to state A. Use the decimal point as an indicator of the output function. Hint, you should define the segments first given the letters. You'll want to create the state machine in VHDL and bring that into another project where you'll tie this together with a frequency divider and anything else you need.

Present State	Future State			
	0 0	0 1	1 0	1 1
A	B	C	E	B
B	D	E	D	A
C	F	G	A	D
D	A	B	F	C
E	C	D	C	G
F	F	G	E	F
G	B	F	D	A

**LAB**

Implement your design on the Altera board using the seven-segment display to depict your present state (use CAPITAL state letters).