EE-313 LAB #1
ALTERA QUARTUS II DESIGN SOFTWARE

BASIC AND COMBINATIONAL LOGIC GATES

1. Purpose: Introduce Altera Quartus II Design Software to simulate the truth tables for combinational logic using block diagrams and a hardware description language (VHDL).

2. Equipment: Desktop with Altera Software
   Altera Quartus II Quick Reference

3. Procedure

   a. Using the Altera Reference guide located on the EE313 website and block diagrams, design, compile, and simulate combinational logic that proves either Boolean Law #2 or Boolean Law #3 (reference textbook – Table 5-2 page 165).

   b. Using VHDL design, compile, and simulate the combinational logic that you chose for part a.

4. Deliverables

   a. Create an entry in your lab notebook as per the course guidelines, with a copy of your combinational block diagram logic (schematic) and its simulation, and a copy of your VHDL code for said combinational logic and its code. You must also demonstrate both simulation outputs to your instructor.

   b. Your lab report within your lab notebook will be written in the following format:

      i. Purpose
      ii. Equipment (if applicable)
      iii. Procedure
      iv. Results
      v. Conclusion

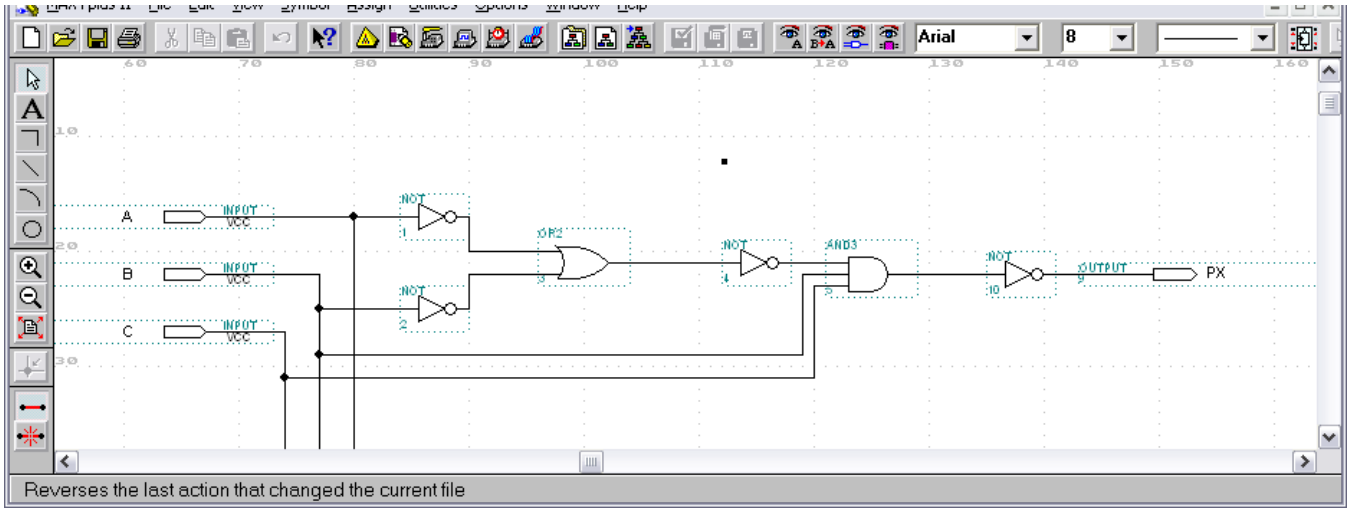

Figure 1: Sample Combinational Logic Gate Diagram

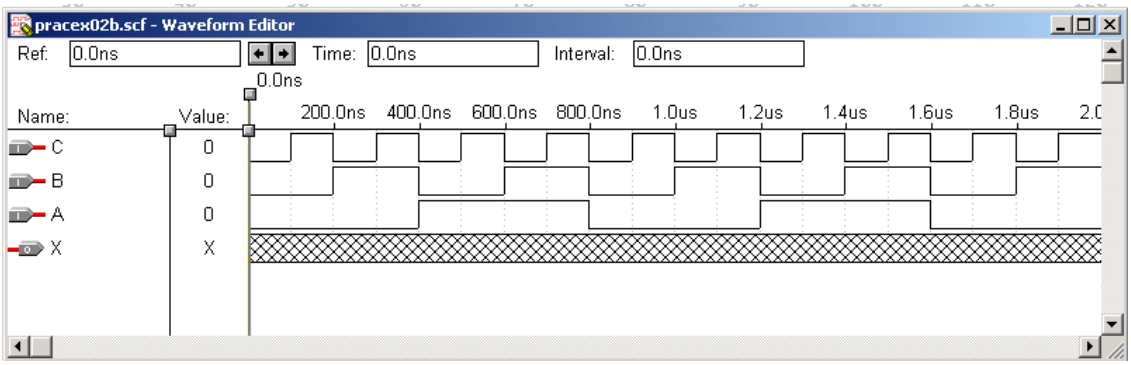

Figure 2: Sample Simulation

Date: January 18, 2008 lab_1b_boolean_law_2_vhdl.vhdProject: lab_1b_boolean_law_2_vhdl

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY lab_1b_boolean_law_2_vhdl IS
    PORT(
        a, b, c, d, e, f: IN std_logic;
        x, y: OUT std_logic);
END lab_1b_boolean_law_2_vhdl;

ARCHITECTURE arc OF lab_1b_boolean_law_2_vhdl IS
    BEGIN
        x<= (a OR (b OR c));
        y<= ((a OR b) OR c);
END arc;
```

USING STANDARD LIBRARY SET OF LOGIC (ALL 313 DESIGNS)

DEFINES INPUT + OUTPUT PORTS

BASIC STRUCTURE OF LOGIC DESIGN

Figure 3: VHDL code