

EE-313 LAB #2
ALTERA QUARTUS II DESIGN SOFTWARE
&
ALTERA PLD BOARD

BASIC AND COMBINATIONAL LOGIC GATES

1. Purpose: Review Altera Quartus II Design Software to simulate the truth tables for combinational logic using block diagrams and a hardware description language (VHDL). Introduce implementation of the logic design in a field-programmable logic array (FPGA).
2. Equipment: Desktop with Altera Software and byteblasterII Parallel Cable
Altera PLD Board
Altera Quartus II Quick Reference

3. Procedure

- a. Using VHDL design, compile and simulate the combinational logic below.

$$X = \overline{(\overline{A\overline{B}D})(B + D)(\overline{A}B + \overline{D})}$$

- b. Using Boolean algebra and DeMorgan theorems, simplify the equation above.

$$X = \underline{\hspace{10em}}$$

- c. Using block diagrams design, compile and simulate your simplified equation.
- d. Implement your block diagram design onto the Altera PLD board.
- e. Using toggles switches and LEDs on the Altera PLD board, demonstrate to the instructor that your logic design on the Altera PLD board provides the same output as your simulated VHDL design.

4. Deliverables

- a. Create an entry in your lab notebook as per the course guidelines, with a copy of your combinational block diagram logic and its simulation, and a copy of your VHDL code for said combinational logic and its code. You must also demonstrate your block diagram logic on the Altera PLD to your instructor.
- b. Your lab report will be written in the following format:
 - i. Purpose
 - ii. Equipment
 - iii. Procedure
 - iv. Results
 - v. Conclusion