EE-313 Boolean Reduction with Quartus II

Rev 01/25/2012

1. ***Purpose***: Learn how to simplify Boolean equations using VHDL and Quartus II.

2. ***Equipment*:** Digital Electronics with Quartus II Book
   Computer with Altera Software
   Altera DE2 Board with power supply and USB cable

3. ***Procedure***:

a. Using the knowledge from the first Quartus II lab, create a new project called lab02_yourlastname with a top level entity called lab02_yourlastname.

NOTE: Ensure you use the following information when creating the project!

Device Family:	Cyclone I
Device:	EP2C35F672C6
EDA simulation Tool Name:	Custom
EDA Simulation Format:	Verilog HDL

b. Create a new VHDL file by selecting **File>New>VHDL File**

NOTE: Recall from your reading that there are three sections to a VHDL file. They are the LIBRARY Declaration which tells the compiler what libraries to be included in the program, the ENTITY Declaration which defines the input and output ports, and the ARCHITECTURE Body which defines the logic function(s) to be implemented.

c. Using Figure 5-32(a) from page 170 of your book as an example, edit the VHDL File you created so that it implements the logic circuit for the following Boolean expression.

$$Y = \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC \qquad [1]$$

NOTE: Things you can expect to change include the *entity_name*, the *output*, and the logic function. If the Boolean equation was $Z = (\overline{A} + B)\overline{C}$ then the VHDL logic function would be *x<=(NOT a OR b) AND NOT c;*.

d. Save the VHDL file as lab02_yourlastname.vhd.

e. Compile the project to verify there are no errors. Fix errors as necessary.

f. Click on **Tools>Netlist Viewers>RTL Viewer**. This will open a window with a schematic of the unreduced implementation of the Boolean expression.

g. Click on **Tools>Netlist Viewers> Technology Map Viewer**. This will open a window with a block diagram of the Boolean expression similar to Figure 1.

h. Double click on the blue box shown in Figure 1. This will show a logic diagram of the circuit that is actually being implemented. Note that it is significantly different than the Boolean expression of Equation 1. Include this logic circuit and the its Boolean equation in your report

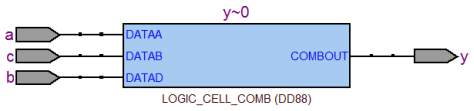

Figure 1 – Technology Map Viewer

```
    y, aa, bb, cc    : OUT std_logic );
lab02_key;

ITECTURE arc OF lab02_key IS
BEGIN
    y<=(NOT a AND B AND NOT C) OR (NOT
    aa<=a;
    bb<=b;
    cc<=c;
```

Figure 2 – VHDL Code Excerpt from step k.

i. Create a new Vector Waveform file to simulate the inputs to your circuit by selecting **File>New>Vector Waveform File**

NOTE: Set the Vector Waveform File End time to 8us and the Grid Size Period to 1us. Refer to the Quartus tutorial Part 20 on page 127 of the book if you forgot how to do this.

j. Add all the inputs and outputs to the Waveform file using selecting **View>Utility_Windows>Node Finder**.

k. Set the period for waveforms a, b, and c to 8, 4, and 2us respectively. Refer to the Altera tutorial from the previous lab if you do not recall how to do this.

NOTE: Ensure you save the simulator file prior to Simulating or you will receive an error notification that no waveform file is selected.

l. Run the simulator tool to verify the reduced circuit has the correct outputs.

m. Add three outputs aa, bb, and cc in your VHDL file next to the y output then add three functions that assign each input to their respective output as shown in Figure 2.

n. Assign the inputs and outputs to pins the pins shown in Tables 1 and 2. Click **Assignments>Pins** to get to the assignment editor. Remember the Pin Number goes in the Location block.

Input	Toggle Switch	Pin No.
a	SW 2	PIN_P25
b	SW 1	PIN_N26
c	SW 0	PIN_N25

Table 1 – Input Pin Assignments

Output	LED	Pin No.
aa	LEDR 2	PIN_AB21
bb	LEDR 1	PIN_AF23
cc	LEDR 0	PIN_AE23
y	LEDG 7	PIN_Y18

Table 2 – Output Pin Assignments

o. Recompile your project and program the Altera Board. Verify the proper operation and demonstrate success to the instructor. Have your lab notebook opened so he can initial for successful completion.

4. *Deliverables*

a. Lab notebook entry per course guidelines.
b. Successful demonstration of the implementation to the instructor.