EE313
LAB 5: MUX DESIGN

1. **Equipment:** Computer with Altera Software and USB Blaster Cable
   Altera DE2 PLD Board
   Altera Quartus II Quick Reference

2. **Purpose:** The purpose of this lab is to:
   a) Demonstrate the operation of a Multiplexer
   b) Learn how to create Symbol Files in Quartus II in order to simplify circuits.
   c) Learn how to utilize the factory PIN assignment file for the DE2 Board.

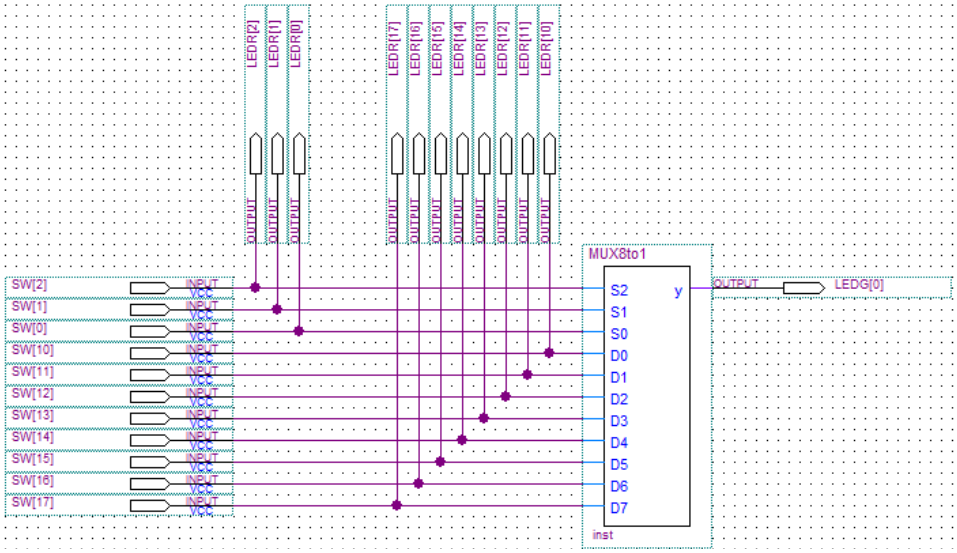

Figure 1: 8-Line Multiplexer Basic Block Diagram

3. **MUX Design and Simulation:**

a. Design an 8-to-1 Multiplexer using logic gates. The control inputs should be labeled S2-S0, the data inputs should be labeled D7-D0 and the output should be labeled Y.

b. Build your circuit using Quartus II software. Your logic circuit can use any combination of gates that results in the proper output for a given input. You may use your book as a reference. D**o NOT use pre-designed ICs (*e.g.* 74150 or 74151)**.

c. Turn your gate-level diagram into a ***Symbol File*** called ***MUX8to1_lastname*** that looks like the MUX8to1 block in Figure 1.

d. Import the PIN Assignment file available on the EE313 website. Refer to the Altera Quick Reference Guide located on the EE313 website to see how this is done. The directions are in section III Method 2 – Standard Naming Nomenclature.

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e. Create the logic circuit shown in Figure 1 using your multiplexer. This is a circuit that connects each input to a toggle switch and a red LED, and the output Y to a green LED. The circuit shall have:

- Each input assigned to the red LED above the associated toggle switch providing the input.
- The output assigned to LEDG[0].
- The inputs S2, S1, S0 connected to toggle switches SW[2], SW[1], and SW[0] respectively.
- The inputs D7 through D0 connected to toggle switches SW[17], SW[16],…,SW[10], respectively.

e. Predict the output of your circuit using Table 1 then simulate your logic circuit using the truth table of Table 1 and include the simulation report in your lab notebook.

f. Program your design to the DE2 board and demonstrate proper operation to the instructor.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	S_2	S_1	S_0	Y Predicted	Y Simulated
0	0	0	0	0	0	0	1	0	0	0		
1	1	1	1	1	1	0	1	0	0	1		
0	0	0	0	0	1	0	0	0	1	0		
1	1	1	1	0	1	1	1	0	1	1		
0	0	0	1	0	0	0	0	1	0	0		
1	1	0	1	1	1	1	1	1	0	1		
0	1	0	0	0	0	0	0	1	1	0		
0	1	1	1	1	1	1	1	1	1	1		
1	1	1	1	1	1	1	0	0	0	0		
0	0	0	0	0	0	1	0	0	0	1		
1	1	1	1	1	0	1	1	0	1	0		
0	0	0	0	1	0	0	0	0	1	1		
1	1	1	0	1	1	1	1	1	0	0		
0	0	1	0	0	0	0	0	1	0	1		
1	0	1	1	1	1	1	1	1	1	0		
1	0	0	0	0	0	0	0	1	1	1		

Table 1: Truth Table for the Multiplexer Logic Circuit in Figure 1

4. **<u>Question for Lab Notebook</u>**

a. How could you use your ***EE_MUX,*** design to implement the following Boolean equation:

$$Y = \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + AB\overline{C} + \overline{A}BC + \overline{A}\overline{B}C$$