

**EE-313 LAB #7**  
**ALTERA QUARTUS II DESIGN SOFTWARE**

## MOD 8 Ripple Up Counter

1. Purpose:

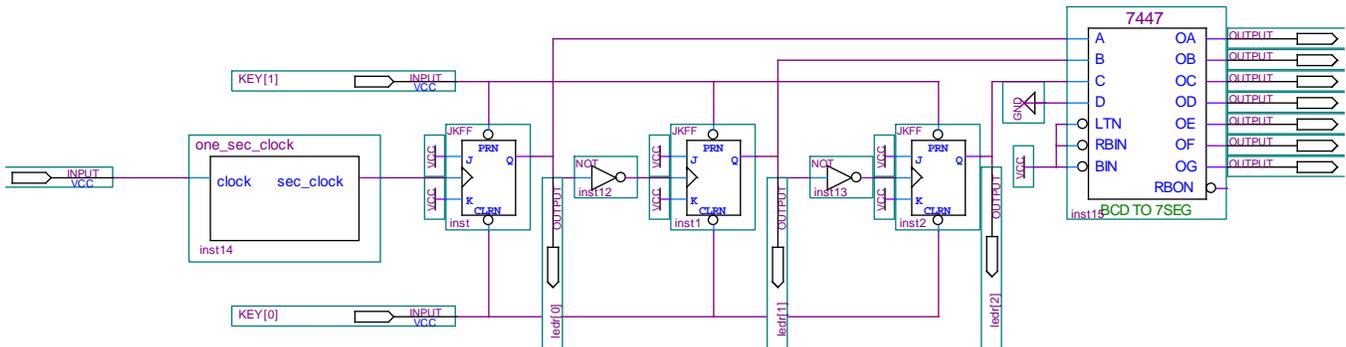
Demonstrate operation of a counter using a Positive Edge Triggered JK Flip Flop  
 Demonstrate use of the 7447 7-Segment Display driver and the 7-Segment Display.  
 Demonstrate operation of Active Low Set and Reset

2. Equipment: Desktop with Altera Software

Altera PLD Board  
 Altera Quartus II Quick Reference

3. Procedure

- a. Create a new Quartus Project called lab07\_lastname.
- b. Download the *one\_sec\_clock.bdf* and *one\_sec\_clock.bsf* files from the EE313 web page and save them in your lab07 project directory.
- c. Create the counter using the given schematic.



Note: Remember that you can find a given symbol by typing its name into the Symbol selector Name block. This project uses 4 new symbols. (VCC, GND, 7447, and ONE\_SEC\_CLOCK)

- d. Download and import the pin assignments file from the EE313 website.
- e. Assign Pins per the following table.

Input	Pin Name
Clock	CLOCK_27
Asynchronous Set	KEY[1]
Asynchronous Reset	KEY[0]
OA,OB,OC,OD, OE, OF, OG	HEX0[0] through HEX0[6]
Q0, Q1, Q2	LEDR[0] through LEDR[2]

- f. Program your Altera board and demonstrate its operation to the Instructor.

4. Deliverables Your lab report shall include:

- a. Block Diagram Schematic
- b. Lessons Learned
- c. Instructor Initial indicating proper demonstration of your project.
- d. Answer how this could be converted to down counter.