10. Buck Chopper Design

The previous sections of this document have hopefully demonstrated that understanding the practical considerations of the components of a buck chopper is critical to a successful design. We uncovered that a capacitor could look like an inductor at high enough frequencies, that a buck chopper FET requires a special "high-side" driver to supply or sink sufficient charge to turn it ON or OFF, that an inductor wrapped on a ferromagnetic core with a distributed air gap will experience copper and core losses, and that a "real" diode does not turn off instantaneously but exhibits a reverse recovery characteristic. These non-ideal component characteristics are then coupled via the buck converter topology and switch control strategy, leading to potential engineering tradeoffs such as efficiency versus size. Our next goal then is to determine a way to manage this interdependency and to logically progress through a buck chopper design.

Clearly we have generated a lot of equations that can be used to estimate the performance of the buck chopper and its components and we are tempted to start "plugging and chugging." Let's step back and propose something a bit more systematic, as illustrated in Figure 10.1. First the design process starts when someone comes to you with *engineering specifications*. For a dc-dc converter a minimal set might include expected input voltage range, desired output voltage and allowable ripple, and maximum output power. These specifications might then couple to *system metrics* such as efficiency, size and weight or energy density, cost, EMI performance, and speed of response. The metrics may manifest as specific bounds, like the converter must fit into a given space within a predefined cabinet, or as with EMI, a bit more holistic (i.e., it must not interfere with nearby communication equipment). By combining these metrics using some weighting system, you can arrive at an *objective function*. The "best" design is then mathematically achieved by maximizing (or minimizing depending how you set it up) the objective function.

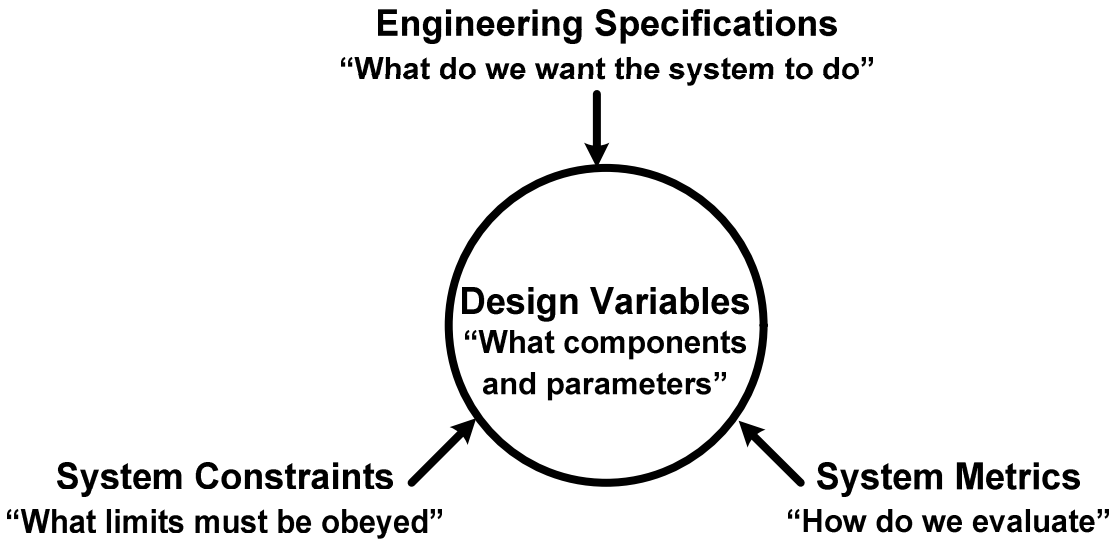

Figure 10.1: Illustration of the Vocabulary of Design

The system metrics are functions of the *design variables* of your system. For the buck chopper, these design variables might be the parameters of the main components (the switch, diode, inductor, capacitor, gate drive, and pwm chip) as well as operational parameters such as the switching frequency and ripple ratio. In terms of the components, the switch can be for instance characterized by its on-resistance, threshold voltage, gate charge characteristic, and breakdown voltage. These parameters are not all independently selectable but will be associated with semiconductor parts that are commercially available. This leads us to the final element of design which we denote as *system constraints*

At one level, you can view system constraints as being *limits of technology* – for example, the smallest practical combination of on-resistance and gate charge for a FET, the maximum permissible flux density for an inductor core, or the highest possible output frequency for a PWM chip. At another level, system constraints might be artificially imposed by limiting the available parts, package types, layout options, etc. Having a good appreciation for the limits of technology and what is reasonable cuts to the fact that design is strongly dependent on both experience and knowledge of the cutting edge. For example, experience might lead one to conclude that a "synchronous" buck chopper can maximize the converter efficiency while knowledge of "silicon-carbide" diodes might inform one as to what are the most efficient parts.

Example 10.1: OK, with that as an introduction let's consider the details of an actual design. To make the example concrete, let's adopt some modest specifications.
We will assume that the input voltage is a 12V lead acid battery whose voltage might be anywhere between 11V and 14V depending on the state of charge. The buck chopper must step that voltage down to a well regulated 6V with no more than a 60mV (1%) peak-to-peak ripple. The buck chopper will supply a load that can draw anywhere from 0 to 1A on average. We could use a linear regulator to achieve the 6V output but at a steep efficiency penalty. For instance at maximum input voltage, we will be dropping $14V - 6V = 8V$ across the regulator and with 1A flowing through it, it will be dissipating 8W and so the efficiency will be a meager $100 \times 6W / \left(6W + 8W\right) = 43\%$. Here we will attempt to do much better.

In terms of constraints, let's assume that we will initially test our design using a proto-board or wire-wrap board and so we choose to not use surface-mount technology. We will further limit our semiconductor device selection to those in the popular and power-dense TO-220 package as the package size matches well with heat sinks that we already have available in the laboratory. We will limit the admissible inductor cores and high-side drivers to ones currently available in stock in the power laboratory. In terms of metrics, we will seek to achieve a full-load efficiency greater than 85% while minimizing the size of inductor and capacitor. This is intentionally nebulous as we have not set forth any sort of way to measure power density or optimize component size. In fact, we have constrained our design to NOT use surface mount technology which is integral to a PC board implementation and shrinking the converter footprint!

The first step in the converter design is to consider admissible devices for both the power switch and the diode. When the diode is conducting, the switch must block the input voltage (plus the diode drop). Ignoring the diode drop for now, this implies that the FET must safely block 14V (the maximum input voltage) and so we apply our rule-of-thumb to estimate a minimal voltage rating

$$V_{rat,\min} = 1.7V_{Block,\max} = 1.7(14V) = 23.8V \tag{10.1}$$

The following are standard available rated FET voltages: 20V, 30V, 40V, 55V, 60V, 75V, 100V, 150V, 200V, and 600V. We are faced with our first engineering judgment decision: Should we go with a 30V rated part or higher? To answer this, we need to consider how the key device attributes, on-resistance and required gate charge, are effected by voltage rating.

The first step is to obtain a list of available FETs. One approach is to go to an electronics technology vendor such as digikey (http://www.digikey.com/) and conduct a search. In the Part Search field at digikey, you could type "mosfet" and it will return with a list of options. Under Discrete Semiconductor Parts, you could then choose "Mosfets – Single" which implies a package with a single device. Now the fun begins as you have a matrix of parameters that you could use to narrow down your choice. For instance here, you might specify FET Type: N-channel, Manufacturer: International Rectifier, Package/case: all of the TO-220 options, and then check the box "In Stock" to ensure that you are finding a part that is available. If you apply the filtering, this will reduce your search field from thousands to about 160 parts. If you click "View Page," you can then see the available parts together with voltage/current rating, typical gate charge, power dissipation, etc. If you click on the digikey part number, you can find links to a data sheet that will contain more specific information as discussed in Section 7. Another "cool" feature of this page is that we can also sort the parts. For instance, directly below the Drain to Source Voltage tag are two arrows which will allow you to sort the parts from high to low voltage or from low to high voltage. This will enable you to start to group potential candidates for our design.

If you do not want to start with the vendor, you might consider going directly to the manufacturer's website. For instance, http://www.irf.com/indexsw.html is home for International Rectifier. Under the Product Line tag, you will find "HEXFET Power MOSFETS." Next you can choose "Discrete HEXFET Power MOSFET – N-Channel" which will identify some 800 potential parts. Fortunately here too is a parameter-based search table which will enable us to refine our search. If we select only devices in a TO-220AB package, our field of choices drops to around 140. If we select "Show All Results," we can start navigating through the table to make some choices. As before, we can use the sorting "arrows" near the top of a column to sort the parts by breakdown voltage, for instance. The manufacturer (IR) provides a lot more information in its parameter table, giving on-resistance at various gate-source voltages, thermal resistance, typical gate charge and gate-drain charge, and the peak continuous current at various case temperatures. To start to get a handle on this let's examine some parts next to one another.

Table 10.1 shows some International Rectifier FET devices that have about the same on-resistance for various breakdown voltages. The table also shows how the typical gate-drain charge Q_{GD} varies. Recall, Q_{GD} is closely connected with the amount of charge required while the device is turning ON or OFF and experiencing switching losses.

Table 10.1: Variation in Required Gate-Drain Charge for FETs with Similar On-Resistance

Part	V_{BRDSS} (V)	I_D at $T_C = 100^\circ C$ (A)	$R_{DS,ON}$ at $T_J = 25^\circ C$ ($m\Omega$)	Q_{GD} typical (nC)
IRFB42N20D	200	30A	55	43
IRF1540N	100	13	52	28.7
IRFZ34E	60	20	42	8.0
IRL1B4343	55	13	50	9.5

The key trend shown in Table 10.1 is that the required charge decreases with decreasing voltage rating, implying that the lower voltage rated devices have less switching losses at a given switching frequency. The product $R_{DS,ON}Q_{GD}$ can loosely be used as a FET figure of merit. The reason that there are no 40V or 30V devices in Table 10.1 is because the on-resistance for these parts is typically much less than $50m\Omega$. We can create another table of parts (Table 10.2) using $25m\Omega$ as the on-resistance value and see the same trend of the required charge decreasing with rated voltage.

Thus we have somewhat answered our first question: use as small of a rated voltage as practical. The caveat to this is that the device must still be sized to handle the switching trajectory. This trajectory is strongly influenced by stray inductance and LC-resonances caused by parasitic components that are not known a priori. For example, stray inductance introduced by input cabling might introduce a large $v = L\frac{dI}{dt}$ transient spike across the switch, especially as we attempt to switch at high frequencies and transition the current quickly (an estimate of between 4nH/cm to 10nH/cm is reasonable for wire). For instance, let's assume that we have 400nH of inductance between the source and switch and that we attempt to turn the switch off by reducing the current from 1A to 0A in 50ns. In this case, $L\frac{\Delta I}{\Delta t} = 400nH\frac{-1A}{50ns}$ predicts that we would get an 8V spike on top of the input voltage that the device must be able to block. Clearly more stray inductance or a greater current transition will aggravate this phenomenon. This effect is in part mitigated by smartly laying out the circuit to minimize the stray inductance. In practice if it remains a problem, a device called a "snubber" is placed around the switch, typically to slow down the switch transitions and control the voltage overshoots. Here we will assume that this has been addressed.

Table 10.2: Variation in Required Gate-Drain Charge for FETs with Similar On-Resistance

Part	V_{BRDSS} (V)	I_D at $T_C = 100^\circ C$ (A)	$R_{DS,ON}$ at $T_J = 25^\circ C$ ($m\Omega$)	Q_{GD} typical (nC)
IRFP4227PBF	200	46	25	23
IRFP3710	100	36	25	17.3
IRFZ34VPBF	60	21	26	12
IRL3303	30	24	26	10

The next question is "what is an appropriate value for the on-resistance?" While the switch is ON, the inductor current is ramping up from its minimum to its maximum values. On average, it equals $I_{L,ave}$. The average conducting switch drop is then

$$V_{SW,ON,ave} = R_{DS,ON} I_{L,ave} \tag{10.2}$$

For a buck chopper in the steady state, the average inductor current must equal the average load current since the capacitor current must have zero average value. So in our design example, this means that $I_{L,ave} = 1A$ and so the magnitude of the average switch drop will equal the magnitude of the on-resistance. What's a reasonable average switch voltage? Probably anything above a couple of volts is getting excessive. For low voltage systems, where output voltages might be down around 1.8 to 3.3V, a much smaller voltage is required to ensure high efficiency. Since conduction losses can be estimated by

$$P_{SW,cond} = I_{L,rms}^2 R_{DS,ON} D \approx I_{L,ave}^2 R_{DS,ON} D \tag{10.3}$$

Where as long as the inductor ripple is small relative to its average value, it does not matter much whether we use the rms or average inductor current. A rule-of-thumb that we would want conduction losses to be no more than 5% of the output power would be reasonable. For our design for a worst case duty cycle, we get

$$R_{DS,ON} < \frac{P_{SW,cond}}{I_{L,ave}^2 D} = \frac{0.05(6W)}{(1A)^2 \frac{6V}{11V}} = 0.55\Omega \tag{10.4}$$

This ballpark estimate shows us that in this design example (low current, low output power), we anticipate that the conduction losses will be small as it is not uncommon to find an on-resistances that is much smaller than half an ohm. Thus we would probably scan the gate-drain charge for the 30V devices (Table 10.3) and choose the smallest value. Here, we might choose the IRF3707Z FET which has $R_{DS,ON} = 9.5m\Omega$ and $Q_{GD} = 3.4nC$. Note, there are smaller $R_{DS,ON}$ values, but this part gives the smallest gate-drain charge and will allow us to consider exploiting higher switching frequencies.

Table 10.3: Selection of International Rectifier 30V FETs

Part	$R_{DS,ON}$ ($m\Omega$) at $V_{GS} = 10V$	Typ. Q_{GD} (nC)	$R_{DS,ON} * Q_{GD}$ ($m\Omega * nC$)
IRF3708	12.0	5.8	69.6
IRF3707Z	9.5	3.4	32.3
IRL3303	26.0	10.0	260.0
IRF3709Z	6.3	6.0	37.8
IRL3713	3.0	37.0	111.0
IRL3103	12.0	11.3	135.6

Upon securing the data sheet for this part, we find that $V_{GS,\max} = 20V$, $T_{j,\max} = 175^{\circ}C$, $R_{\Theta,jc} = 2.653^{\circ}C/W$, and $V_{GS,TH} \approx 1.8V$. Also, we can collect information on the on-resistance temperature variation and typical gate charge requirements as shown in Figure 10.2. Here, if we consider operation at a junction temperature of $120^{\circ}C$ as a worst case, we see that the on-resistance will increase to about $1.4 \times (9.5m\Omega) = 13.3m\Omega$. From the gate charge curve, we see that $V_{Miller} \approx 3V$, $Q_{GS2} \approx 3.8nC - 2.5nC \approx 1.3nC$ (this is the amount of gate charge required after V_{GS} has exceeded the threshold voltage and up to the Miller plateau), $Q_{GD} = 8.2nC - 3.8nC = 4.4nC$ (the amount of charge required while at the Miller Plateau), and $Q_G \approx 11nC$ (this is the overall required gate charge when $V_{GS} = 5V$ with a blocking voltage of 15V).

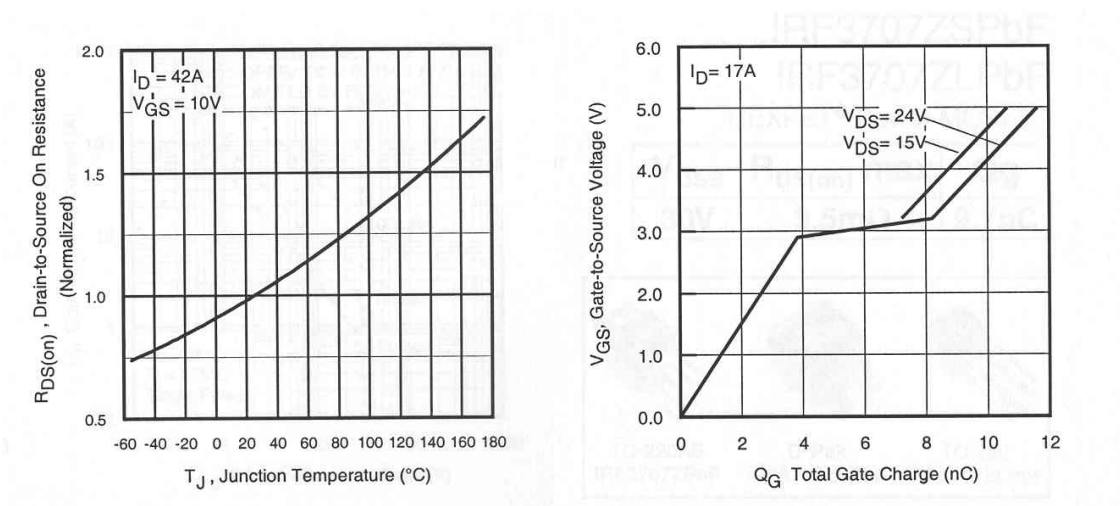

Figure 10.2: IRF3707Z Data Sheet Graphs

Our next decision involves the choice of driver and the driver voltage. The boot-strap high-side drivers introduced in Section 5 are not attractive choices for this particular FET because the required gate-source voltage is so low ($\sim 5V$). The IR2125 for instance requires a supply voltage of at least 10V so these chips are poorly matched to this application. We will find that there are other vendors that supply drivers. For instance,

Linear Technology produces the LTC1693 high-side driver which has an allowable input voltage down to 4.5V. The only downside of this component is that it is only available in surface mount packages meaning that an adaptor chip might be required to evaluate the design on a proto-board. To enable us to continue on with this design example, we will assume that the driver that we ultimately choose will have a maximum current capability on the order of about 1A. Further, a gate-source voltage of 8V is reasonable (it will not force us to supply too much excess gate charge as shown in Figure 10.2) so based on

$$R_{DR} + R_{Gext} > \frac{V_{DR}}{\left| I_{DR,\max} \right|} \tag{10.5}$$

we will insist that $R_{DR} + R_{Gext} = 8\Omega$. At this point, we can start estimating the FET turn-on and turn-off times so we can then consider switching losses. For turn-on, we need to estimate the current rise time and voltage fall time using

$$t_{IR} = \frac{Q_{GS2}\left(R_{DR} + R_{Gext}\right)}{V_{DR} - \left(\frac{V_{GS,TH} + V_{Miller}}{2}\right)} = \frac{1.3nC \times 8\Omega}{8V - \left(\frac{1.8V + 3V}{2}\right)} = 1.86ns \tag{10.6}$$

$$t_{VF} = \frac{Q_{GD}\left(R_{DR} + R_{Gext}\right)}{V_{DR} - V_{Miller}} = \frac{4.4nC \times 8\Omega}{8V - 3V} = 7.04ns \tag{10.7}$$

Recall, these expressions are based on “linearized” voltage/current trajectories which are approximations of the actual more complex variations. The “typical” switch turn-on time is then estimated as

$$T_{SW,ON} = t_{IR} + t_{VF} = 8.9ns \tag{10.8}$$

Simulation will better estimate this value but in the initial design phase, this at least gets us into the ballpark. We can later test our design or refine our calculations with the help of simulation. Now for the turn-off time, we need to estimate the voltage rise time and current fall time using

$$t_{VR} = \frac{Q_{GD}\left(R_{DR} + R_{Gext}\right)}{V_{Miller}} = \frac{4.4nC \times 8\Omega}{3V} = 11.73ns \tag{10.9}$$

$$t_{IF} = \frac{Q_{GS2}\left(R_{DR} + R_{Gext}\right)}{\left(\frac{V_{GS,TH} + V_{Miller}}{2}\right)} = \frac{1.3nC \times 8\Omega}{\left(\frac{1.8V + 3V}{2}\right)} = 4.33ns \tag{10.10}$$

The “typical” switch turn-off time is then estimated as

$$T_{SW,OFF} = t_{VR} + t_{IF} = 16.06ns \tag{10.11}$$

When the FET turns ON, the current must ramp up from zero to the minimum value of inductor current while the blocking voltage is the sum of the input voltage and the conducting diode drop. Thus, the turn-on switching losses may be expressed by

$$P_{FET,SW,ON} = \frac{\frac{1}{2}V_{DS,OFF}I_{D,ON}T_{SW,ON}}{T_{SW}} = \frac{1}{2}\left(V_{IN} + V_F\right)I_{L,\min}T_{SW,ON}f_{SW} \tag{10.12}$$

When the FET turns OFF, the current must ramp down from the maximum inductor current and the blocking voltage must build to the sum of the input and diode drop so the power loss is estimated by

$$P_{FET,SW,OFF} = \frac{\frac{1}{2}V_{DS,OFF}I_{D,ON}T_{SW,OFF}}{T_{SW}} = \frac{1}{2}\left(V_{IN} + V_F\right)I_{L,\max}T_{SW,OFF}f_{SW} \tag{10.13}$$

In (10.12) and (10.13) we need information about both the inductor current ripple and the diode forward voltage drop so let's make some initial choices.

Since we are at low voltages ($11V < V_{IN} < 14V$ and $V_{OUT} = 6V$), the diode must be able to block $V_{IN} - V_{SW}$. As we have seen with such low current, the switch drop is negligible so the diode (worst case) must block ~14V. If we apply our rule of thumb, then the rated diode blocking voltage should be $1.7 \times 14V \approx 24V$. At this low voltage, Schottky diodes are a possibility and will be preferred because of their low forward voltage drop and negligible reverse recovery. To search for them at digikey type "diode" in the Part Search field. Then under Discrete Semiconductor Products, select "Diodes, Rectifiers – Single." In the parameter table, select Diode/Rectifier Type: Schottky and Package/Case: TO-220AB and TO-220AC. As always check the box that indicates that the part must be in stock. This will narrow your search to some 60 devices with voltage ratings ranging from 120V down to 15V. The average current flowing in the diode will be

$$I_{D,ave} = \frac{T_{SW} - t_{ON}}{T_{SW}} I_{L,ave} = \left(1 - D\right)I_{L,ave} \tag{10.14}$$

Ignoring non-idealities as an initial stab, the lowest duty cycle occurs at maximum input voltage or $D = \frac{6}{14} = 0.429$. Thus, $I_{D,ave} \approx 0.571A$. When the diode is ON, the diode will be carrying 1A on average. We would like to choose the device with as low of a forward diode drop at that current level as possible. In this case, most of the devices will have a voltage drop on the order of 0.3V at such a low current. Let's choose part number MBR735PBF (Figure 10.3). We can then inspect the reverse voltage versus reverse current characteristic which shows that with 15V reverse bias and a junction temperature

of $125^{\circ}C$ (probably way too hot for this application), we would anticipate a worst-case reverse current of no more than 1mA. The diode blocking losses could be estimated as $14V \times 1mA \approx 14mW$.

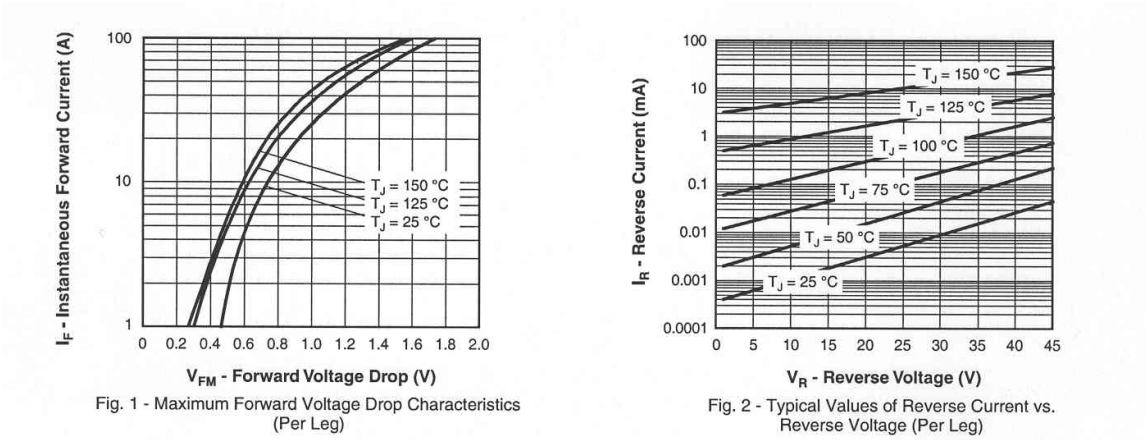

Figure 10.3: Diode Data Sheet Information

OK, now we need to specify our ripple ratio or the nominal value of the inductor ripple current. If you review the discussion in Section 1, a ripple ratio in the range of $0.2 < r < 0.6$ was attractive in that it was not too small as to require excessive inductance and not too big to require excessive ripple current capability from the capacitor. Here is a good opportunity to perform some iterative design and sweep the options. Let's consider the lower end which will correspond to the largest amount of inductance ($r = \frac{\Delta I_L}{I_{L,ave,\max}} = 0.2$). Thus for a maximum average current of 1A, this corresponds to a peak-to-peak ripple of 0.2A. Therefore the maximum inductor current will be 1.1A and the minimum inductor current will be 0.9A.

The switching losses can then be estimated as

$$P_{FET,SW,ON} = \frac{1}{2}\left(V_{IN} + V_F\right) I_{L,\min} T_{SW,ON} f_{SW} = \frac{1}{2}\left(14 + 0.3\right) \times 0.9A \times 8.9ns \times f_{SW} \quad (10.15)$$

$$P_{FET,SW,ON} = 57.27 \times 10^{-9} \times f_{SW} \quad (10.16)$$

And

$$P_{FET,SW,OFF} = \frac{1}{2}\left(V_{IN} + V_F\right) I_{L,\max} T_{SW,OFF} f_{SW} = \frac{1}{2}\left(14 + 0.3\right) \times 1.1A \times 16.06ns \times f_{SW} \quad (10.17)$$

$$P_{FET,SW,OFF} = 126.3 \times 10^{-9} \times f_{SW} \quad (10.18)$$

Therefore the estimated total turn-on and turn-off switching losses become

$$P_{FET,SW} = P_{FET,SW,ON} + P_{FET,SW,OFF} = 183.6\times10^{-9}\times f_{SW} \tag{10.19}$$

If we arbitrarily wish to limit our switching losses to no more than 5% of the rated output power, we can impress an upper switching frequency limit as

$$f_{SW,\max} = \frac{0.05\times6}{183.6\times10^{-9}} \approx 1.6MHz \tag{10.20}$$

We can also impose a constraint on the amount of the period that we allow for switching. Let's say we want no more than 2% of the period to be switching time. Thus,

$$T_{SW,ON} + T_{SW,OFF} < 0.02\times T_{SW} \tag{10.21}$$

or

$$f_{SW,\max} < \frac{0.02}{T_{SW,ON} + T_{SW,OFF}} = \frac{0.02}{8.9ns + 16.06ns} \approx 801kHz \tag{10.22}$$

Other factors that will limit the maximum frequency are the PWM chip capability, the inductor core losses, and the additional time required for FET turn-on and turn-off delay. So in our initial go, let's be ultra-conservative and choose $f_{SW} = 200kHz$. This would be another parameter that you could further investigate.

Before proceeding to the inductor and capacitor designs, let's estimate the conduction losses. To do this we have to estimate the diode and switch drop.

$$V_{SW,ON,ave} = R_{DS,ON} I_{L,ave} \approx 13.3m\Omega\times1A = 13.3mV \tag{10.23}$$

$$V_{F,ave} \approx 0.3V \tag{10.24}$$

Note this order of magnitude difference in voltage drop indicates why it is attractive to try to replace the diode (even a Schottky diode) by a FET if possible (this gives rise to what is called the "synchronous" buck chopper topology. Next we can more accurately estimate the duty cycle,

$$D = \frac{V_{out,ave} + V_F}{V_{IN} - V_{SW} + V_F} = \frac{6V + 0.3V}{14V - 0.0133V + 0.3V} = 0.441 \tag{10.25}$$

The switch and diode conduction losses could then be estimated as

$$P_{FET,Cond} = DI_{L,ave}^2 R_{DS,ON} = 0.441 \times 1 \times 0.0133 = 6mW \tag{10.26}$$

$$P_{Dio,Cond} = (1-D)V_F I_{L,ave} = (1-0.441) \times 0.3V \times 1A = 168mW \tag{10.27}$$

These values will change slightly as we sweep the range of input voltages but should be representative. Clearly, the order of magnitude difference in voltage drop leads to a stark difference between the conduction losses. Next we can start designing the main buck inductor. We will determine the largest required critical inductance by using the duty cycle at maximum input voltage, so

$$L_{crit} = \frac{(V_{out,ave} + V_F)(1-D)}{rf_{SW} I_{L,ave,\max}} = \frac{(6+0.3)(1-0.441)}{0.2 \times 200k \times 1} = 88\mu H \tag{10.28}$$

OK, to determine the smallest admissible core that will not experience excessive drop in permeability, we need to calculate the peak inductor energy

$$E_L = \frac{1}{2} L I_{pk}^2 = \frac{1}{2} \times 88\mu H \times \left(1A + \frac{0.2A}{2}\right)^2 = 53.24\mu J = 0.05324mJ \tag{10.29}$$

Table 3.3 indicates that the 0.4” core is too small, while the 0.8” core ought to be adequate. The larger cores would also work but they will obviously weigh more, take up more space, and be more costly. The advantage of the larger cores is that they will permit fewer turns because of the larger A_L value. The 125-mu 0.8” Kool Mu core has $A_L = 68mH/1000turn$ with other physical parameters listed in Table 3.4. Thus the initial calculation of the required turns is,

$$N = 1000\sqrt{\frac{88\mu H}{68mH}} = 36turn \tag{10.30}$$

Next we will need to determine how much to bump that value up to account for changes in the permeability due to a DC bias.

$$H_{A/m} = \frac{NI_{Lave}}{l_{tot}} = \frac{36 \times 1A}{5.09cm/(100cm/m)} = 707A/m \tag{10.31}$$

or in oersted

$$H_{oersted} = \frac{4\pi}{1000} H_{A/m} = 8.88oe \tag{10.32}$$

Figure 3.4 then predicts a change in permeability of about 0.9 so we can then re-evaluate the turns to be

$$N = 1000\sqrt{\frac{L_2}{A_L}}\sqrt{\frac{\mu_{eff\,1}}{\mu_{eff\,2}}} = 36\sqrt{\frac{1}{0.9}} = 38turn \qquad (10.33)$$

To determine the appropriate wire gauge, we first evaluate the maximum anticipated inductor RMS current using

$$I_{L,rms} = \sqrt{I_{L,ave}^2 + \left(\frac{\Delta I_L}{\sqrt{12}}\right)^2} = \sqrt{(1A)^2 + \left(\frac{0.2A}{\sqrt{12}}\right)^2} = 1.002A \qquad (10.34)$$

If we use Table 3.1 and employ a current density of $600A/cm^2$, #24 wire is adequate. It has $0.0843\Omega/m$ with a $0.0566cm$ diameter. The fill factor must be checked to ensure that the number of turns will fit in the core window (where the window area is found in Table 3.4).

$$K_U = \frac{Area(Used)}{Area(Available)} = \frac{(turns)\frac{\pi}{4}D_{wire}^2}{Area_{window}} = \frac{(38turns)\frac{\pi}{4}(0.0566cm)^2}{1.14cm^2} = 0.083 \qquad (10.35)$$

A fill factor that is less than 0.5 will be adequate and we should not have any problem winding the core.

We can next estimate the inductor losses by first calculating the length of conductor required to achieve the 38 turns. The length per turn is found on the core data sheet as 2.33cm/turn, so

$$R_L = (2.33cm/turn)(38turn)(1m/100cm)(0.0843\Omega/m) = 0.075\Omega \qquad (10.36)$$

The copper losses are then computed to be

$$P_{L,cu} = I_{L,rms}^2 R_L = (1.002A)^2(0.075\Omega) = 0.0753W \qquad (10.37)$$

The inductor core losses are dependent on both the current ripple and the frequency. We can evaluate the peak change in field intensity by

$$\Delta H_{pk} = \frac{N\left(\frac{\Delta I_L}{2}\right)}{l_{tot}} = \frac{38turn(0.1A)}{5.09cm \times \frac{1m}{100cm}} = 74.7A/m \qquad (10.38)$$

We can then convert this to a change in flux density

$$\Delta B_{pk,T} = \mu_{eff}\,\mu_o \Delta H_{pk} = (125\times 0.9)\left(4\pi\times 10^{-7} H/m\right)(74.7A/m) = 0.0106T \quad (10.39)$$

Converting to Kilogauss

$$\Delta B_{pk,kG} = 10\Delta B_{pk,T} = 10\times 0.0106 = 0.106kG \quad (10.40)$$

Finally we use Figure 3.6 or the accompanying formula to estimate the core loss density

$$D_L = \Delta B_{pk,kG}^2 f_{SW,kHz}^{1.46} = (0.106)^2 (200)^{1.46} = 25.71mW/cm^3 \quad (10.41)$$

The volume of core material is available from its data sheet, so

$$P_{L,core} = D_L V_{core} = \left(25.71mW/cm^3\right)\left(1.15cm^3\right) = 29.6mW \quad (10.42)$$

We can then find the total inductor losses

$$P_L = P_{L,cu} + P_{L,core} = 75.3mW + 29.6mW = 104.9mW \quad (10.43)$$

With the rated output power of the converter being 6W, the inductor losses are 1.75% which is reasonable. It would be interesting to see the effect on overall losses of increasing the switching frequency. Certainly FET switching losses will linearly increase; however, the inductor size will get smaller, implying fewer turns and less copper losses. The inductor core losses will most like go up since there is a very strong frequency dependency in (10.41). This is the nature of design: determining what is important and then tweaking the design parameters to optimize this metric.

To complete the current design, we need to determine the appropriate capacitance and choose some devices. Let's start with the voltage ripple requirement of 60mV. This will impose a minimum capacitance given the inductor ripple current and the switching frequency according to

$$C_{\min} = \frac{\Delta I_L}{8 f_{SW} \Delta V_{Cpp}} = \frac{0.2}{8\times 200k\times 0.06} = 2.08\mu F \quad (10.44)$$

Recall though for improved transient performance, we might like to balance the peak energy in the inductor with the energy in the capacitor so

$$\frac{1}{2} L I_{L,pk}^2 = \frac{1}{2} C V_{out}^2 \quad (10.45)$$

or

$$C = L\left(\frac{I_{L,pk}}{V_{out}}\right)^2 = 88\mu H \times \left(\frac{1.1A}{6V}\right)^2 = 2.96\mu F \tag{10.46}$$

If it is critical to further reduce overshoot, this value of capacitance can be increased. Specifically if you would like to guarantee an overshoot of about 10%, you would need to scale this value by five. The maximum required capacitor RMS current is found from

$$I_{C,rms} = \frac{\Delta I_L}{\sqrt{12}} = \frac{0.2A}{\sqrt{12}} = 57.7mA \tag{10.47}$$

For such a low value of capacitance, a ceramic capacitor might be the best choice but let's revisit aluminum electrolytics and consider the FC series that was discussed in Section 2. The smallest capacitor available at a rated 25V is a $10\mu F$ (the 25V ensures that even if the input voltage gets applied the capacitor, it will be OK). This capacitor has a maximum ripple current rating of 65mA and a DF of 0.14. If you wish to have a bit more margin on the ripple current, you can consider a 50V $10\mu F$ capacitor that has a maximum RMS ripple current of 125mA with a DF of 0.1. Let's choose that part. We can next estimate the ESR using

$$R_{esr} \approx \frac{DF}{\omega C} \approx \frac{0.1}{2\pi \times 200k \times 10 \times 10^{-6}} = 0.008\Omega \tag{10.48}$$

We can estimate the maximum power dissipated in the capacitor by

$$P_{Cap} = I_{C,rms}^2 R_{esr} = \left(57.7mA\right)^2\left(0.008\Omega\right) = 26.6\mu W \tag{10.49}$$

which is fairly insignificant compared to switching, conduction, and inductor losses. If we assume a lead inductance of 20nH and minimal connection inductance, we can estimate the resonant frequency of the capacitor using

$$f_{C,res} = \frac{1}{2\pi\sqrt{L_{esl}C}} = \frac{1}{2\pi\sqrt{20\times10^{-9}\left(10\times10^{-6}\right)}} = 356kHz \tag{10.50}$$

Since this is greater than our switching frequency of 200kHz, the capacitor will in fact look like a capacitor at the switching frequency. The last item that we need to evaluate for our capacitor is the voltage ripple due to the ESR, here we use

$$\Delta V_{out,pp,esr} = \Delta I_L R_{esr} = \left(0.2A\right)\left(0.008\Omega\right) = 1.6mV \tag{10.51}$$

which is much smaller than the specified 60mV ripple, so we are OK. We would probably add some high-frequency capable ceramic capacitors in parallel with our

electrolytic capacitor to improve the high-frequency performance and help with noise immunity.

The final element of loss that we have not quantified is that associated with the driver. This loss will be divided between the driver chip and the external gate resistance, but we will lump them together for now. The loss depends on the total gate charge supplied to the FET. Since with 8V applied, we are somewhat out of the characteristic shown in Figure 10.2, we will need to estimate this value. Here, we will propose 18nC. The power can then be estimated from

$$P_{DR,ON} = V_{DR} Q_G f_{SW} = 8V \times 18nC \times 200kHz = 28.8mW \tag{10.52}$$

This shows that if we can reduce this loss by considering a lower drive voltage but how would that have effected our switching times? If we summarize our component losses in Table 10.4 (by returning to (10.19) to update our switching loss calculation), we find that at maximum output power (6W) our converter experiences on the order of 360mW of losses, leading to an efficiency estimate of $\frac{6W}{6W + 0.36W} \times 100 = 94\%$. There will be one further source of loss that is not documented here that is due to the required 8V auxiliary DC supply (required by the driver), but this accounting at least points us in the direction of where we can improve our design or how we can go about trading off losses.

Table 10.4: Design 1 Power Loss Analysis

Component	Type of Loss	Value
FET	Conduction	6mW
	Switching	37mW
Diode	Conduction	168mW
	Blocking	14mW
Driver	Gate Charge	28.8mW
Inductor	Copper	75.3mW
	Core	29.6mW
Capacitor	ESR	0.026mW

The final step in our design process is to revisit the cooling requirements of the power semiconductor devices. In this case, neither device is dissipating more than 1W so no heat sink should be required. Since the thermal resistance junction-to-ambient for a TO-220 package is on the order of $62^\circ C/W$ and considering the maximum junction temperature as $150^\circ C$ and the maximum ambient temperature as $50^\circ C$, we can estimate the maximum permissible power dissipation as $\frac{150^\circ C - 50^\circ C}{62^\circ C/W} = 1.6W$.

Example 10.2: Let's consider a second design that might be relevant for an emerging automotive application. We want to step down a nominal 42V battery down to 14V. At 14V out, we want the converter to provide 10A and have the output voltage ripple be smaller than 100mV. To simplify the closed-loop control, we will want to maintain the converter in continuous conduction mode (CCM) for most of its operating mode and thus specify a ripple ratio of 0.2. With this choice the converter will stay in CCM from 14W to 140W output.

Step 1: Specify the power switch

Using our rule of thumb for voltage rating $V_{rat} \approx 1.7V_{\max}$ and since the maximum voltage across the switch will be approximately the input voltage, $V_{rat} \approx 1.7 \times 42V \approx 71.4V$. We could use a 75V MOSFET, but to provide a bit more margin, we will bump up the rating to 100V. With the duty cycle being approximately $D \approx \frac{V_{out}}{V_{in}} \approx \frac{14V}{42V} = 0.333$ and if we wish to limit the conduction losses of the switch to less than 5% of the rated output power, we get a bound on the on-resistance of $R_{DS,ON} < \frac{P_{SW,cond}}{I_{L,ave}^2 D} = \frac{0.05(120W)}{(10A)^2\, 0.333} = 0.18\Omega$.

If we review a list of available power IR FETS rated for 100V, this is not a very restrictive value. Let's suppose that we select the IRFB59N10D FET that has $R_{DS,ON} = 25m\Omega$ at room temperature, a typical $Q_{GD} = 36nC$, and a maximum threshold voltage of 5.5V. The maximum junction temperature is $175^\circ C$ and $R_{\Theta,jc} = 0.75^\circ C/W$. Graphs from the data sheets are listed in Figure 10.4. At $T_J = 125^\circ C$, the on-resistance increases by a factor of about 1.7 to $42.5m\Omega$. The Miller plateau is approximately 7V, while $Q_{GS2} \approx 24nC - 18nC \approx 6nC$ and $Q_{GD} \approx 55nC - 24nC \approx 31nC$. The total gate charge with $V_{GS} = 12V$ is about 83nC (all derived from Figure 10.4).

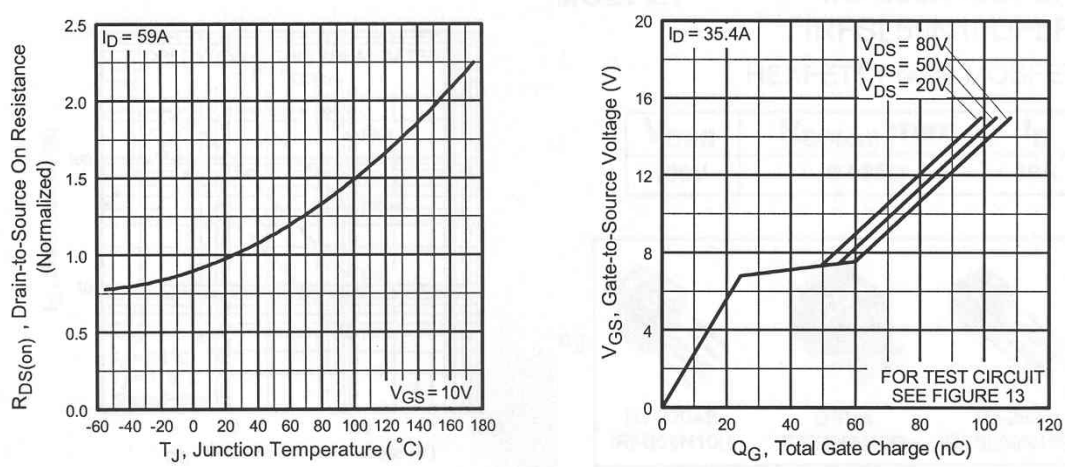

Figure 10.4: IRFB59N10D Data Sheet Graphs

Step 2: Select the Gate Driver, Gate Driver Voltage, and external gate resistance

Let's suppose we choose the IRS2110 high/low-side gate driver that has a nominal maximum output current of 2A and a power supply under-voltage lockout value of 9.6V. We will choose a supply voltage of 12V which seems reasonable given the FET gate charge characteristic and is safely above the gate driver under-voltage level.

$$R_{DR} + R_{Gext} > \frac{V_{DR}}{\left|I_{DR,\max}\right|} = \frac{12V}{2A} = 6\Omega \tag{10.53}$$

Step 3: Estimate the FET switching times.

For turn-on

$$t_{IR} = \frac{Q_{GS2}\left(R_{DR} + R_{Gext}\right)}{V_{DR} - \left(\frac{V_{GS,TH} + V_{Miller}}{2}\right)} = \frac{6nC \times 6\Omega}{12V - \left(\frac{5.5V + 7V}{2}\right)} = 6.26ns \tag{10.54}$$

$$t_{VF} = \frac{Q_{GD}\left(R_{DR} + R_{Gext}\right)}{V_{DR} - V_{Miller}} = \frac{31nC \times 6\Omega}{12V - 7V} = 37.2ns \tag{10.55}$$

The "typical" switch turn-on time is then estimated as

$$T_{SW,ON} = t_{IR} + t_{VF} = 43.5ns \tag{10.56}$$

For turn-off

$$t_{VR} = \frac{Q_{GD}\left(R_{DR} + R_{Gext}\right)}{V_{Miller}} = \frac{31nC \times 6\Omega}{7V} = 26.6ns \tag{10.57}$$

$$t_{IF} = \frac{Q_{GS2}\left(R_{DR} + R_{Gext}\right)}{\left(\frac{V_{GS,TH} + V_{Miller}}{2}\right)} = \frac{6nC \times 6\Omega}{\left(\frac{5.5V + 7V}{2}\right)} = 5.76ns \tag{10.58}$$

The "typical" switch turn-off time is then estimated as

$$T_{SW,OFF} = t_{VR} + t_{IF} = 32.4ns \tag{10.59}$$

Step 4: Select the Main Diode

The main diode must be able to block the input voltage, 42V, thus it should also have a rating of at least 75V. The average diode current is $I_{D,ave} = (1-D)I_{L,ave} \approx (1-0.333)\times 10A = 6.67A$ with a peak current of $I_{D,pk} = I_{L,ave} + \frac{\Delta I_L}{2} = 10A + \frac{2A}{2} = 11A$. Since this blocking voltage is below 150V, we should first consider a Schottky diode. One candidate is the V20100SG-E3/4WGI-ND which is rated for 100V, 20A, in a TO-220AB package, with characteristics shown in Figure 10.5. With a current of 10A flowing through this device, Figure 10.5 shows that the forward voltage drop at $125^{\circ}C$ is about 0.6V. Further at that temperature, while the device is blocking, the reverse current that flows will be on the order of 3mA (while blocking 42V).

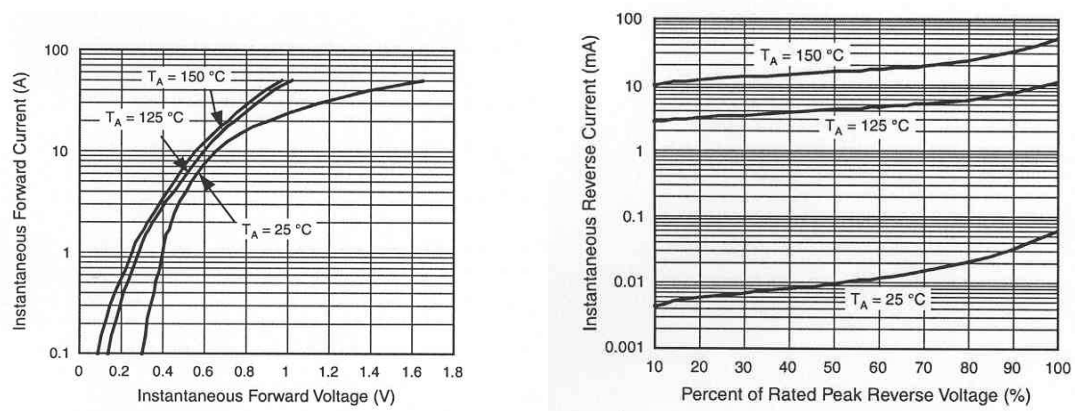

Figure 10.5: Diode Data Sheet Information

Step 5: Estimate the FET and Diode Conduction Losses

Next we can estimate the duty cycle at full power (the device voltage drops will decrease at lower output powers),

$$D = \frac{V_{out,ave} + V_F}{V_{IN} - V_{SW} + V_F} = \frac{14V + 0.6V}{42V - (10A \times 0.0425\Omega) + 0.6V} = 0.346 \qquad (10.60)$$

The switch and diode conduction losses could then be estimated as

$$P_{FET,Cond} = DI_{L,ave}^2 R_{DS,ON} = 0.346 \times 10^2 \times 0.0425 = 1.47W \qquad (10.61)$$

$$P_{Dio,Cond} = (1-D)V_F I_{L,ave} = (1-0.346) \times 0.6V \times 10A = 3.92W \qquad (10.62)$$

Step 6: Estimate a maximum switching frequency based on the total FET losses

The switching losses are

$$P_{FET,SW,ON} = \frac{1}{2}\left(V_{IN} + V_F\right) I_{L,\min} T_{SW,ON} f_{SW} = \frac{1}{2}\left(42 + 0.6\right) \times 9A \times 43.5ns \times f_{SW} \quad (10.63)$$

$$P_{FET,SW,ON} = 8.34 \times 10^{-6} \times f_{SW} \quad (10.64)$$

and

$$P_{FET,SW,OFF} = \frac{1}{2}\left(V_{IN} + V_F\right) I_{L,\max} T_{SW,OFF} f_{SW} = \frac{1}{2}\left(42 + 0.6\right) \times 11A \times 32.4ns \times f_{SW} \quad (10.65)$$

$$P_{FET,SW,OFF} = 7.59 \times 10^{-6} \times f_{SW} \quad (10.66)$$

Therefore the estimated total turn-on and turn-off switching losses become

$$P_{FET,SW} = P_{FET,SW,ON} + P_{FET,SW,OFF} = 15.93 \times 10^{-6} \times f_{SW} \quad (10.67)$$

What is the total power that this part can handle? Well, since $R_{\Theta,jc} = 0.75^{\circ}C/W$, $R_{\Theta,cs} \approx 0.5^{\circ}C/W$, and a typical large heat sink offers $R_{\Theta,sa} \approx 2.5^{\circ}C/W$, then if we choose $T_{J,\max} = 125^{\circ}C$ and a maximum ambient temperature of $T_{A,\max} = 40^{\circ}C$ we can estimate the total power dissipation as

$$P_{diss} = \frac{T_{J,\max} - T_{A,\max}}{R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}} = \frac{125 - 40}{0.75 + 0.5 + 2.5} = 22.7W \quad (10.68)$$

Since our conduction losses are a modest 1.5W, we have up to 20W to comfortably waste on switching losses, but that value is probably much larger than what we want!

If we wish to limit FET switching losses to no more than 5% of rated output power (~7W) then

$$f_{SW,\max} = \frac{0.05 \times 140}{15.93 \times 10^{-6}} \approx 439kHz \quad (10.69)$$

We can also impose a constraint on the amount of the period that we allow for switching. Let's say we want no more than 2% of the period to be switching time. Thus,

$$T_{SW,ON} + T_{SW,OFF} < 0.02 \times T_{SW} \quad (10.70)$$

or

$$f_{SW,\max} < \frac{0.02}{T_{SW,ON} + T_{SW,OFF}} = \frac{0.02}{43.5ns + 32.4ns} \approx 264kHz \tag{10.71}$$

Our PWM chip can comfortably handle 264kHz. Let's provide ourselves with a bit more margin and choose 200kHz.

<u>Step 7:</u> Specify the Inductor

First we evaluate the critical inductance

$$L_{crit} = \frac{\left(V_{out,ave} + V_F\right)\left(1-D\right)}{rf_{SW}I_{L,ave,\max}} = \frac{\left(14+0.6\right)\left(1-0.346\right)}{0.2\times 200k\times 10} = 23.9\mu H \tag{10.72}$$

OK, to determine the smallest admissible core that will not experience excessive drop in permeability, we need to calculate the peak inductor energy

$$E_L = \frac{1}{2}LI_{pk}^2 = \frac{1}{2}\times 23.9\mu H\times\left(10A + \frac{2A}{2}\right)^2 = 1.45mJ \tag{10.73}$$

Table 3.3 indicates that the 1.3" core is too small, while the 2.25" core ought to be adequate. The 125-mu 2.25" Kool Mu core has $A_L = 156mH/1000turn$ with the remainder of its relevant parameters given in Table 3.4. Thus the initial calculation of the required turns is,

$$N = 1000\sqrt{\frac{23.9\mu H}{156mH}} = 12.4turns \tag{10.74}$$

Next we will need to determine how much to bump that value up to account for changes in the permeability due to a DC bias.

$$H_{A/m} = \frac{NI_{Lave}}{l_{tot}} = \frac{12.4\times 10A}{14.3cm/\left(100cm/m\right)} = 867A/m \tag{10.75}$$

or in oersted

$$H_{oersted} = \frac{4\pi}{1000}H_{A/m} = 10.9oe \tag{10.76}$$

Figure 3.4 then predicts a change in permeability of about 0.85 so we can then re-evaluate the turns to be

$$N = 1000\sqrt{\frac{L_2}{A_L}}\sqrt{\frac{\mu_{eff\,1}}{\mu_{eff\,2}}} = 12.4\sqrt{\frac{1}{0.85}} = 14turns \qquad (10.77)$$

To determine the appropriate wire gauge, we first evaluate the maximum anticipated inductor RMS current using

$$I_{L,rms} = \sqrt{I_{L,ave}^2 + \left(\frac{\Delta I_L}{\sqrt{12}}\right)^2} = \sqrt{(10A)^2 + \left(\frac{2A}{\sqrt{12}}\right)^2} = 10.02A \qquad (10.78)$$

If we use Table 3.1 and employ a current density of $600A/cm^2$, #14 wire is adequate. It has $0.00827\Omega/m$ with a $0.1714cm$ diameter. The fill factor must be checked to ensure that the number of turns will fit in the selected core window (the window area is found in Table 3.4).

$$K_U = \frac{Area(Used)}{Area(Available)} = \frac{(turns)\frac{\pi}{4}D_{wire}^2}{Area_{window}} = \frac{(14turns)\frac{\pi}{4}(0.1714cm)^2}{9.48cm^2} = 0.034 \qquad (10.79)$$

A fill factor that is less than 0.5 is adequate and we should not have any problem winding the core.

We can next estimate the inductor losses by first calculating the length of conductor required to achieve the 14 turns. The length per turn is found on the core data sheet as 5.30cm/turn, so

$$R_L = (5.30cm/turn)(14turn)(1m/100cm)(0.00827\Omega/m) = 0.00614\Omega \qquad (10.80)$$

The copper losses are then computed to be

$$P_{L,cu} = I_{L,rms}^2 R_L = (10.02A)^2(0.00614\Omega) = 0.616W \qquad (10.81)$$

The inductor core losses are dependent on both the current ripple and the frequency. We can evaluate the peak change in field intensity by

$$\Delta H_{pk} = \frac{N\left(\frac{\Delta I_L}{2}\right)}{l_{tot}} = \frac{14turn(1A)}{14.3cm \times \frac{1m}{100cm}} = 97.9A/m \qquad (10.82)$$

We can then convert this to a change in flux density by

$$\Delta B_{pk,T} = \mu_{eff}\mu_o \Delta H_{pk} = (125\times 0.85)(4\pi\times 10^{-7} H/m)(97.9A/m) = 0.0131T \quad (10.83)$$

Converting to Kilogauss

$$\Delta B_{pk,kG} = 10\Delta B_{pk,T} = 10\times 0.0131 = 0.131kG \quad (10.84)$$

Finally we use Figure 3.6 or the accompanying formula to estimate the core loss density

$$D_L = \Delta B_{pk,kG}^2 f_{SW,kHz}^{1.46} = (0.131)^2 (200)^{1.46} = 39.27mW/cm^3 \quad (10.85)$$

The volume of core material is available from its data sheet, so

$$P_{L,core} = D_L V_{core} = (39.27mW/cm^3)(20.65cm^3) = 811mW \quad (10.86)$$

We can then find the total inductor losses

$$P_L = P_{L,cu} + P_{L,core} = 616mW + 811mW = 1.427W \quad (10.87)$$

With the rated output power of the converter being 140W, the inductor losses are 1% which is reasonable.

<u>Step 8:</u> Specify the Capacitor

To complete the current design, we need to determine the appropriate capacitance and choose a component or components. Let's start with the voltage ripple requirement of 100mV. This will impose a minimum capacitance given the inductor ripple current and the switching frequency according to

$$C_{\min} = \frac{\Delta I_L}{8 f_{SW}\Delta V_{Cpp}} = \frac{2}{8\times 200k\times 0.1} = 12.5\mu F \quad (10.88)$$

Recall though for transient performance, we might like to balance the peak energy in the inductor with the energy in the capacitor so

$$\frac{1}{2}LI_{L,pk}^2 = \frac{1}{2}CV_{out}^2 \quad (10.89)$$

or

$$C = L\left(\frac{I_{L,pk}}{V_{out}}\right)^2 = 23.9\mu H \times \left(\frac{11A}{14V}\right)^2 = 14.75\mu F \tag{10.90}$$

As mentioned previously, if you would like to guarantee an overshoot of about 10%, you would need to scale this value by five. The maximum required capacitor RMS current is found from

$$I_{C,rms} = \frac{\Delta I_L}{\sqrt{12}} = \frac{2A}{\sqrt{12}} = 577mA \tag{10.91}$$

With a 42V input voltage, we would like at least a 50V rated capacitor and might be better served with a 100V device. If we scan the FC-series 100V capacitors, we see that the closest standard available part is $22\mu F$, but this device only has a ripple capability of 260mA with a dissipation factor (DF) of 0.07. The $10\mu F$ device has a ripple capability of 114mA so we would have to place six of these in parallel to meet our specification. Instead, let's choose to place three $22\mu F$ capacitors in parallel to achieve a ripple capability of 780mA (note, a single $68\mu F$ capacitor gives a maximum ripple capability of only 599mA). We can next estimate the ESR using

$$R_{esr} \approx \frac{DF}{\omega C} \approx \frac{1}{3}\left(\frac{0.07}{2\pi \times 200k \times 22 \times 10^{-6}}\right) = 0.00085\Omega \tag{10.92}$$

where the $\frac{1}{3}$ out front is due to the fact that we are placing three $22\mu F$ capacitors in parallel. We can estimate the maximum power dissipated in the capacitor by

$$P_{Cap} = I_{C,rms}^2 R_{esr} = \left(577mA\right)^2\left(0.00085\right) = 283\mu W \tag{10.93}$$

which is fairly insignificant compared to switching, conduction, and inductor losses. If we assume a lead inductance of 20nH, with three capacitors in parallel, the effective inductance is reduced to 6.67nH. The capacitors in parallel add, so we have $66\mu F$ of capacitance. We can estimate the resonant frequency of the capacitor bank using

$$f_{C,res} = \frac{1}{2\pi\sqrt{L_{esl}C}} = \frac{1}{2\pi\sqrt{6.67\times10^{-9}\left(66\times10^{-6}\right)}} = 240kHz \tag{10.94}$$

Since this is greater than our switching frequency of 200kHz, the capacitor will in fact look like a capacitor at the switching frequency. If we wish to further increase the resonant frequency, we could either place more parts in parallel or decrease the total parallel capacitance. The last item that we need to evaluate for our capacitor is the voltage ripple due to the ESR, here we use

$$\Delta V_{out,pp,esr} = \Delta I_L R_{esr} = (2A)(0.00085\Omega) = 1.7mV \tag{10.95}$$

which is much smaller than the specified 60mV ripple, so we are OK. We would probably add some high-frequency capable ceramic capacitors in parallel with our electrolytic capacitor to improve the high-frequency performance and help with noise immunity.

The final element of loss that we have not yet quantified is that associated with the driver. This loss will be divided between the driver chip and the external gate resistance, but we will lump them together for now. The loss depends on the total gate charge supplied to the FET. Since with 12V applied we found from Figure 10.4 that $Q_G \approx 83nC$, the power can then be estimated from

$$P_{DR,ON} = V_{DR} Q_G f_{SW} = 12V \times 83nC \times 200kHz = 0.2W \tag{10.96}$$

If we summarize our component losses in Table 10.5 (by returning to (10.67) to update our switching loss calculation at 200kHz), we find that at maximum output power (140W) our converter experiences on the order of 10.4W of losses, leading to an efficiency estimate of $\frac{140W}{140W + 10.4W} \times 100 = 93\%$. Again since we will require a 12V DC supply for our driver and PWM chip, there will also be a small amount of loss introduced there as well. Layout will also influence the switch trajectory and can also negatively influence the switching losses, so you might view the 93% as being in the "ballpark."

Table 10.5: Design 2 Summary of Losses at Full Power

Component	Type of Loss	Value
FET	Conduction	1.47W
	Switching	3.19W
Diode	Conduction	3.92W
	Blocking	0.126W
Driver	Gate Charge	0.2W
Inductor	Copper	0.616W
	Core	0.811W
Capacitor	ESR	0.170mW

<u>Step 9:</u> Heat Sink Specification

The last element of this design is to consider cooling requirements. Since both the diode and FET are dissipating more than 1W (about what a TO-220 package can safely handle), an external heat sink is required. If we use the above dissipation values as worst case and use the published junction-case thermal resistances, we can establish the largest permissible heat sink thermal resistance for each part.

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss,FET}} - R_{\Theta,jc} - R_{\Theta,cs} = \frac{125^{\circ}C - 40^{\circ}C}{4.66W} - 0.75^{\circ}C/W - 0.5^{\circ}C/W = 17^{\circ}C/W \quad (10.97)$$

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss,Dio}} - R_{\Theta,jc} - R_{\Theta,cs} = \frac{125^{\circ}C - 40^{\circ}C}{4.05W} - 2.2^{\circ}C/W - 0.5^{\circ}C/W = 18.3^{\circ}C/W \quad (10.98)$$

In either case the heat sink HS278-ND with thermal resistance of $16.7^{\circ}C/W$ ought to be adequate (shown in Figure 10.6).

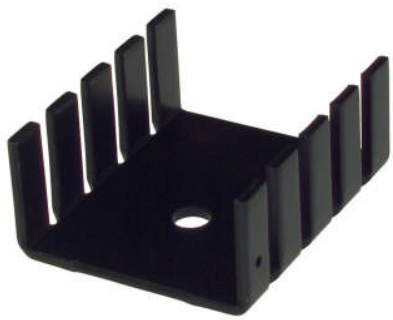

Figure 10.6: Photo of HS278-ND Heat Sink