1.0 Buck Converter Operation

A power electronic converter uses semiconductor devices to transform power from one form (DC or AC) into another form (DC or AC). It accomplishes this by causing the circuit topology to change by virtue of turning ON and OFF the semiconductor devices. A buck converter is a specific type of dc-dc power electronic converter whose goal is to *efficiently step down* DC voltage to a lower level with minimal ripple. Practical applications are illustrated in Figure 1.1 where, for example, a buck chopper might interface between the varying output voltage of a storage battery and a sensitive piece of electronics such as a microprocessor. Typically the buck converter employs feedback to regulate the output voltage in the presence of load changes. This improvement in performance over voltage dividers and regulators comes at the cost of additional components and complexity. In the remainder of this handout, we will examine the characteristics of the buck chopper and derive relationships and tools necessary to properly specify the components required to implement a desired design.

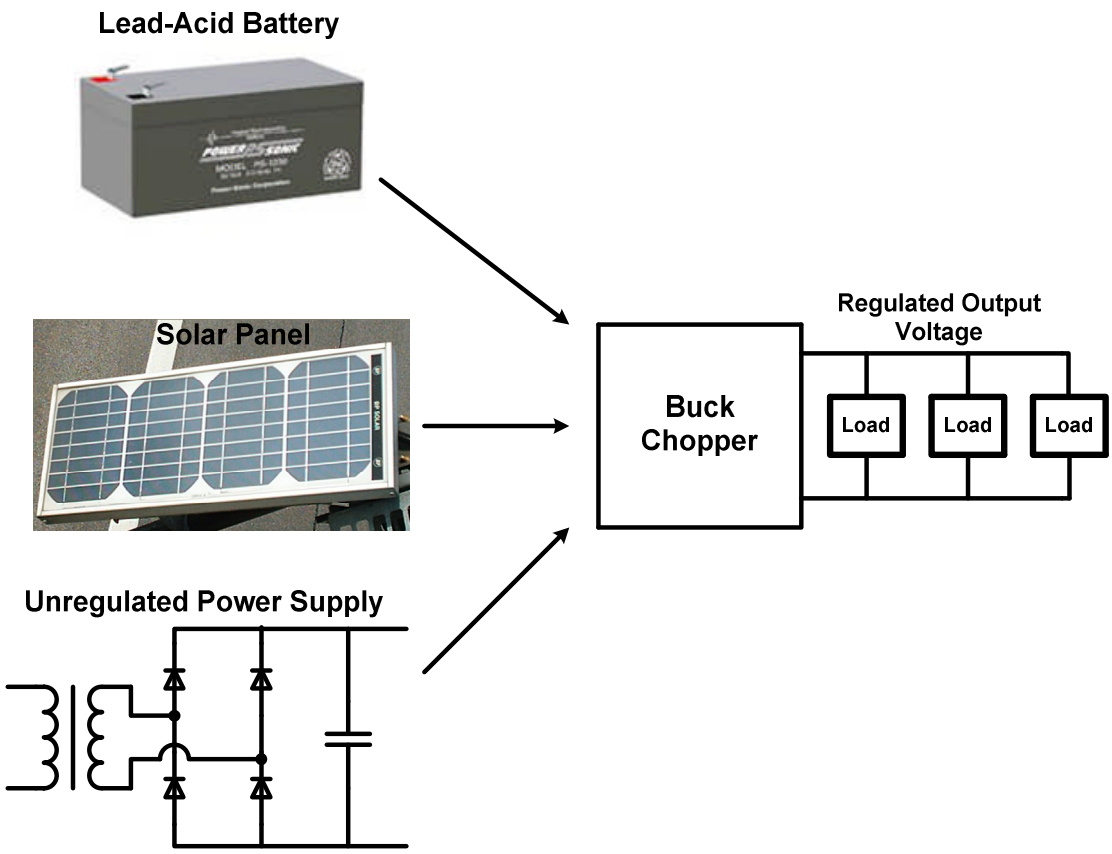
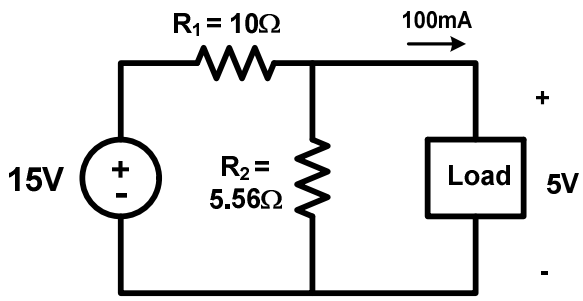


Figure 1.1: Potential Buck Chopper Applications

Example 1.1: Consider an application that requires 0-100mA at 5V. Assume that you only have access to a +15V power supply. Let's consider 3 potential solutions.

Solution #1: Voltage Divider
Consider that we design the following voltage divider circuit, where the desired maximum load is in essence a $5V/100mA = 50\Omega$ resistor. For smaller load currents, the equivalent resistor will be larger.

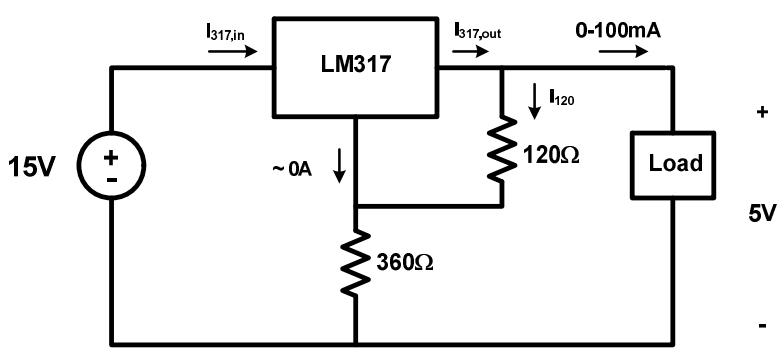


The design shown achieves 5V across the load for the maximum load current requirement. As the load current drops, the output voltage will increase to 5.36V at no load (0A). Thus there are two issues with the voltage divider: (1) for a changing load, you cannot always get what you want and (2) the divider resistors must be smaller than the load resistance to ensure that the output voltage does not change significantly with load. These issues manifest themselves in an efficiency quandary. KVL reveals that there must be 15V – 5V = 10V across the 10Ω resistor and, therefore, we are drawing 1A from the 15V supply. Thus our efficiency is a paltry

$$\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{5V\left(100mA\right)}{15V\left(1A\right)} \times 100 = \frac{0.5W}{15W} \times 100 = 3.33\%$$

We are not effectively using our input voltage energy. In fact we are wasting $\left(1A\right)^2 10\Omega = 10W$ in the one resistor and $\left(5V\right)^2 / 5.56\Omega = 4.5W$ in the other. Let's consider a more elegant solution

Solution #2: Linear Voltage Regulator
We can implement the following circuit design using an integrated circuit chip.



The LM317 works by establishing 1.25V across the 120Ω resistor, hence $I_{120} = 1.25V/120\Omega = 10.4mA$. With zero current leaving the bottom of the chip, this means that there is $10.4mA \times 360\Omega = 3.75V$ across the bottom resistor, so that there is always 1.25V + 3.75V = 5V across the load (within the current capability of the chip). We can establish the output current of the chip using KCL:

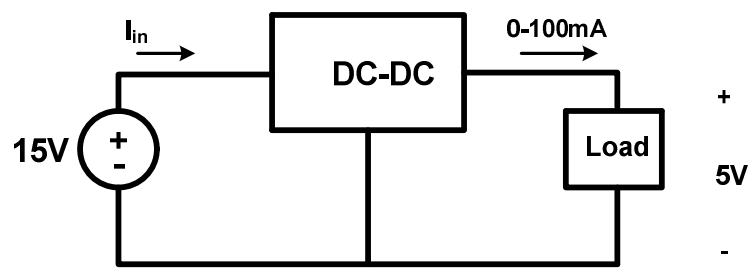
$$I_{317,out} = 100mA + 10.4mA = 110.4mA$$

Then applying KCL to the entire LM317 chip, the input current must be the same or $I_{317,in} = I_{317,out} = 110.4mA$. We can then calculate the efficiency as

$$\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{5V(100mA)}{15V(110.4mA)} \times 100 = \frac{0.5W}{1.656W} \times 100 = 30.2\%$$

Thus we are still inefficiently using the power supply energy and wasting $1.656W - 0.5W = 1.156W$ in the chip and resistors. This leads us to the final solution.

<u>Solution #3:</u> Buck Chopper
Assume that we will learn that a typical dc-dc converter efficiency is in the range of 85-95%. Let's assume here that we can achieve 92%, how does this impact our system?



We can determine the required input power from

$$P_{in} = \frac{P_{out}}{\eta} = \frac{0.5W}{0.92} = 0.543W$$

Thus we are only "wasting" 0.543W - 0.5W = 0.043W and the required input current has dropped to $I_{in} = P_{in}/V_{in} = 0.543W/15V = 36.2mA$. Had our input source been a battery, then we would be drawing far less current with this solution, implying that we would be increasing the battery life.

So now that we have the context of why we currently do not have a good way of efficiently converting to a lower DC voltage, we need to dig into the details of how a buck chopper accomplishes this!

The buck chopper circuit contains semiconductor switches (think transistors and diodes) that will enable us to "chop" up a given voltage to create a waveform with a new and controllable average value. To explain how this happens, consider the circuit shown in Figure 1.2 where we have two *ideal* (zero voltage drop) switches S_1 and S_2. The circuit is controlled in a periodic fashion as shown in Figure 1.3 where T_{SW} is called the *switching period*. Part of a switching cycle switch S_1 is closed while S_2 is open ($V_{S2} = V_{IN}$); the remainder of the cycle S_2 is closed while S_1 is open ($V_{S2} = 0V$).

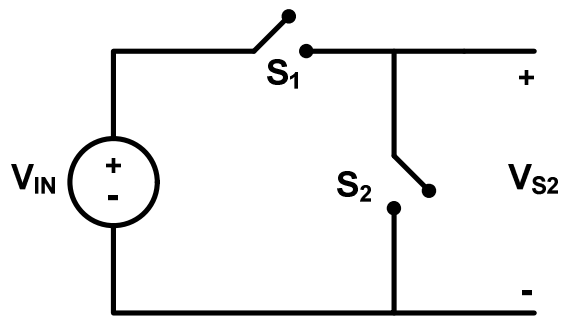


Figure 1.2: Buck Chopper Switch Building Block

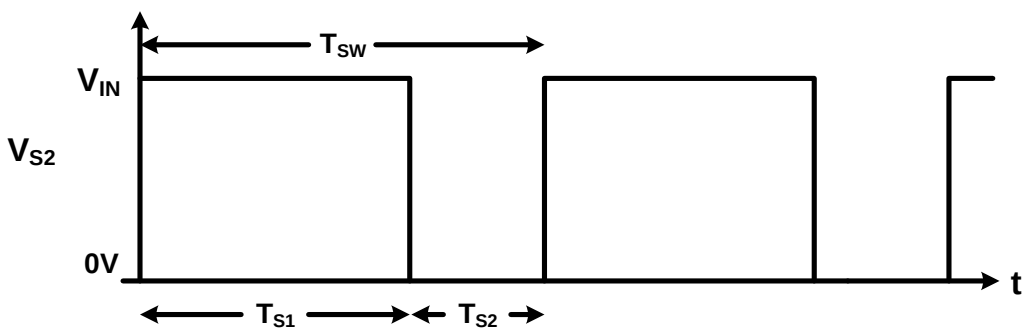


Figure 1.3: Output Voltage for Figure 1 Circuit

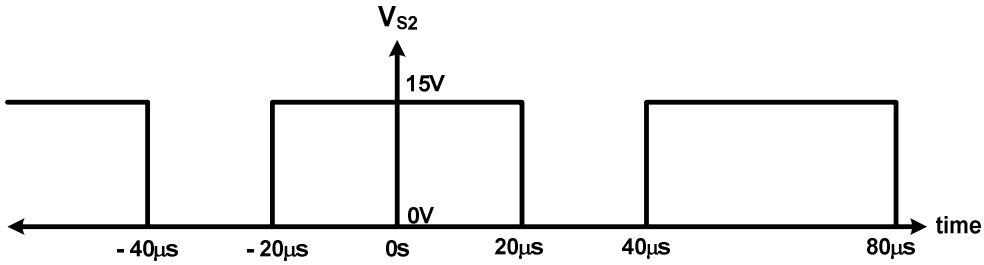
The average value of V_{S2} in Figure 1.3 is found from

$$V_{S2,ave} = \frac{1}{T_{SW}} \int_0^{T_{SW}} V_{S2}(t)dt = \frac{T_{S1}V_{IN} + T_{S2}0}{T_{SW}} = DV_{IN} \tag{1.1}$$

In Equation (1.1) we have introduced the "*duty cycle*" D as being the ratio of the switch S_1 ON-time (T_{S1}) to the switching period (T_{SW}). The V_{S2} voltage waveform is attractive in that we can regulate the average value by changing D, but the large ripple or voltage variation would be unacceptable for most sensitive electronic applications. As a consequence, we would like to "filter" this waveform to extract the average value (DC

component) while attenuating the fundamental ($f_{SW} = \frac{1}{T_{SW}}$) and its harmonics ($2f_{SW}$, $3f_{SW}$, $4f_{SW}$, …).

<u>Example 1.2</u>: Given the following "chopped" waveform (centered for your convenience), establish the first three terms of the Fourier series.



We can observe that the waveform has even symmetry (so the Fourier series will only contain cosines) and the period is given by $T_{SW} = 40\mu s - (-20\mu s) = 60\mu s$. This corresponds to a fundamental frequency of $1/60\mu s = 16.7kHz$. The DC value is found from

$$V_{S2,DC} = \frac{2}{60\mu s}\int_0^{30\mu s} V_{S2}(t)dt = \frac{2}{60\mu s}\int_0^{20\mu s} 15dt = \frac{2}{60\mu s}(15t)\Big|_0^{20\mu s} = 10V$$

The fundamental, second harmonic, and third harmonic amplitudes are found from

$$V_{S2,1} = \frac{4}{60\mu s}\int_0^{20\mu s} 15\cos\left(\frac{2\pi}{60\mu s}t\right)dt = \frac{60}{60\mu s}\times\frac{60\mu s}{2\pi}\times\sin\left(\frac{2\pi}{60\mu s}t\right)\Bigg|_0^{20\mu s} = 8.27V$$

$$V_{S2,2} = \frac{4}{60\mu s}\int_0^{20\mu s} 15\cos\left(2\frac{2\pi}{60\mu s}t\right)dt = \frac{60}{60\mu s}\times\frac{60\mu s}{4\pi}\times\sin\left(2\frac{2\pi}{60\mu s}t\right)\Bigg|_0^{20\mu s} = -4.13V$$

$$V_{S2,3} = \frac{4}{60\mu s}\int_0^{20\mu s} 15\cos\left(3\frac{2\pi}{60\mu s}t\right)dt = \frac{60}{60\mu s}\times\frac{60\mu s}{6\pi}\times\sin\left(3\frac{2\pi}{60\mu s}t\right)\Bigg|_0^{20\mu s} = 0V$$

Thus, we can write the Fourier series for this waveform as

$$V_{S2} = 10V + 8.27V\cos(2\pi\times 16.7kHz\times t) - 4.13V\cos(2\pi\times 33.3kHz\times t) + \ldots$$

This exposes that the waveform has a DC component, the fundamental at 16.7kHz, and the second harmonic at 33.3kHz. Due to the waveform symmetry, the third harmonic is not present. The fourth harmonic at 66.7kHz has an amplitude of 2.07V. The key here is that we want to filter these signals out so that only the DC component remains.

This requires a low-pass filter and we propose the circuit shown in Figure 1.4 where R represents the applied load. Clearly the circuit is low-pass since at low frequencies ($\omega \to 0$) the inductor (ωL) appears as a short and the capacitor ($1/\omega C$) is an open and the input passes through to the output. At high frequencies ($\omega \to \infty$), the inductor looks like an open and the capacitor a short and the input is blocked from the output.

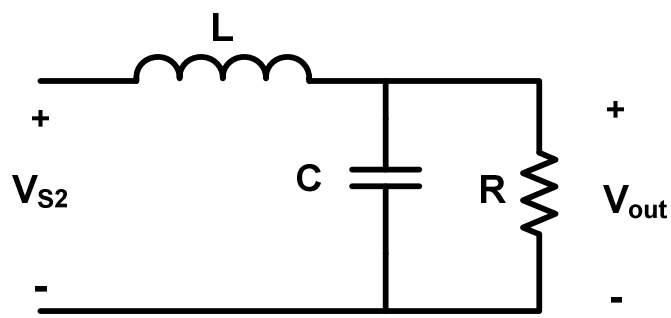


Figure 1.4: Low-Pass Filter within a Buck Chopper

The transfer function for this circuit is given by

$$\frac{V_{out}(s)}{V_{S2}(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} = \frac{1}{LCs^2 + \frac{L}{R}s + 1} \tag{1.2}$$

If we assume that the denominator roots are complex (the usual situation), the approximate straight-line frequency response magnitude characteristic will have a corner frequency at $\omega_o = \frac{1}{\sqrt{LC}}$ as shown in Figure 1.5. The fundamental switching frequency (in rad/s) relates to the switching period and switching frequency (in Hz) by

$$\omega_{SW} = \frac{2\pi}{T_{SW}} = 2\pi f_{SW} \tag{1.3}$$

Note in Figure 1.5 that it is desirable for the switching frequency to appear a couple of decades higher than ω_o so that the ripple in V_{S2} is sufficiently attenuated. In this example, the ripple at ω_{SW} is reduced by -80dB or by a factor of 1×10^{-4} absolute. What this is starting to uncover is that there is a direct relationship between the choice of switching frequency and the selection of L and C.

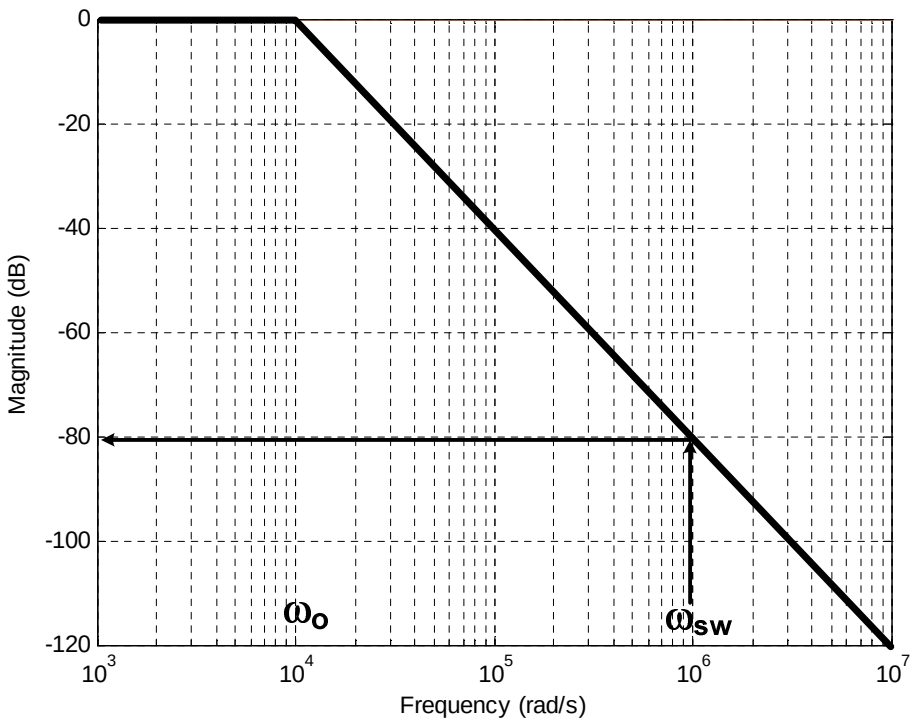


Figure 1.5: Approximate Frequency Response Magnitude Plot for Buck Output Filter

Now the filter discussion is useful in uncovering that $\omega_{SW} >> 1/\sqrt{LC}$, but it does not provide guidance in how to divide up the contributions of L and C nor does it concretely link to desired figures of merit like output ripple voltage or inductor ripple current. Thus we push onward by analyzing the combination of the circuits from Figures 1.2 and 1.4 as shown in Figure 1.6. Here we have replaced switch S_2 by an ideal diode. Thus when switch S_1 opens, any positive inductor current will clamp the diode ON and it will remain on as long as positive current can flow or up until S_1 recloses (thereby reverse biasing the diode and turning it OFF).

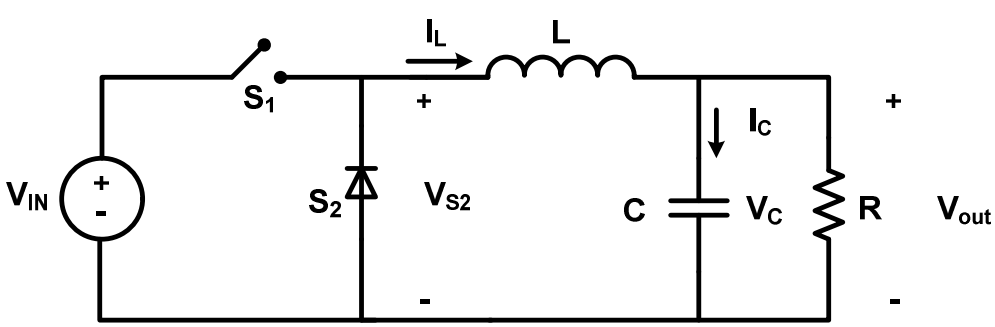


Figure 1.6: Buck Chopper

The preliminary analysis of this circuit utilizes the following assumptions

- C is large enough that the output voltage ripple is small relative to its average value;
- L is large enough to ensure that the inductor current stays positive for the switching period (this is referred to as continuous conduction mode or CCM) – this ensures that when the switch is OFF, the diode must be ON;
- All components are initially assumed ideal – we will eventually find that S_1, S_2, L and C all have parasitic elements that must be considered in properly identifying parts;
- The circuit is in the steady state – implying that all waveforms are in fact periodic, ensuring that they have the same value at the beginning and end of a switching period.

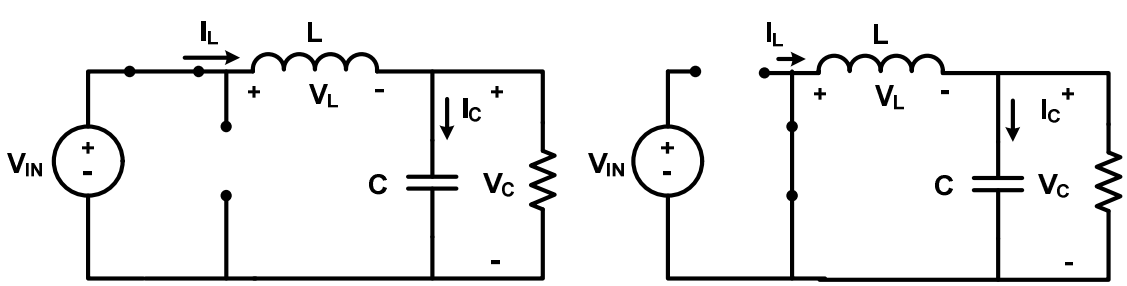
Owing to the second assumption, the circuit will have two admissible states as shown in Figure 1.7: switch closed and diode OFF or switch open and diode ON. Next we will use the first assumption to deduce the wave-shape of the inductor current. First let's re-express the amount of time that the switch and diode are conducting in terms of the duty cycle D

$$T_{S1} = \frac{T_{S1}}{T_{SW}} T_{SW} = DT_{SW} \tag{1.4}$$

$$T_{S2} = T_{SW} - T_{S1} = T_{SW} - DT_{SW} = (1-D)T_{SW} \tag{1.5}$$

If the output voltage ripple is very small, then we can assume that the output voltage is constant at its average value, $V_{out,ave}$. Thus when switch S_1 is ON (Figure 1.7a) we can use KVL to derive an expression for the inductor voltage

$$V_L = L\frac{dI_{L,ON}}{dt} = V_{IN} - V_{out,ave} \tag{1.6}$$



a. S_1 ON & S_2 OFF b. S_2 ON & S_1 OFF

Figure 1.7: Two Valid Topological States for a Buck Chopper in CCM

Since both V_{IN} and $V_{out,ave}$ are constant, the derivative is a constant and we can replace it by the "change" in current over the "change" in time. Thus (1.6) becomes

$$\frac{\Delta I_{L,ON}}{\Delta t_{ON}} = \frac{V_{IN} - V_{out,ave}}{L} \tag{1.7}$$

Substituting for the amount of time that S_1 is ON (Equation (1.4)) and solving for the change in current, we get

$$\Delta I_{L,ON} = \left(\frac{V_{IN} - V_{out,ave}}{L} \right) D T_{SW} \tag{1.8}$$

Note that since $V_{out,ave} < V_{IN}$, the current is linearly building during this interval as shown in Figure 1.8. When switch S_1 is OFF and the diode is conducting, the circuit shown in Figure 1.7b governs and now the inductor voltage is given by

$$\mathrm{V_L} = L \frac{dI_{L,OFF}}{dt} = 0 - V_{out,ave} \tag{1.9}$$

Since we are still assuming that the output voltage is constant, the derivative is again constant so we can rewrite (1.9) as

$$\frac{\Delta I_{L,OFF}}{\Delta t_{OFF}} = \frac{-V_{out,ave}}{L} \tag{1.10}$$

Substituting (1.5) for the amount of time that the diode is assumed to be ON (Equation 1.5) yields

$$\Delta I_{L,OFF} = \frac{-V_{out,ave}}{L} (1 - D) T_{SW} \tag{1.11}$$

Now the current is linearly decreasing (the derivative is negative) as shown in Figure 1.8. For the circuit to be in the steady state and all variables periodic implies that the inductor current must return to the same value at the end of the cycle (indicated here as $I_{\min}$) or mathematically that

$$\Delta I_{L,ON} + \Delta I_{L,OFF} = 0 \tag{1.12}$$

If we substitute (1.8) and (1.11), we find that

$$\left(\frac{V_{IN}-V_{out,ave}}{L}\right)DT_{SW}-\frac{V_{out,ave}}{L}\left(1-D\right)T_{SW}=0 \tag{1.13}$$

After canceling L and T_{SW} , we are left with

$$DV_{IN}-DV_{out,ave}-V_{out,ave}+DV_{out,ave}=0 \tag{1.14}$$

or simply that

$$V_{out,ave}=DV_{IN} \tag{1.15}$$

which thankfully is what we found from our low-pass filter considerations. As shown in Figure 1.8, the steady-state inductor current signal is triangular with the peak-to-peak current designated by ΔI_L .

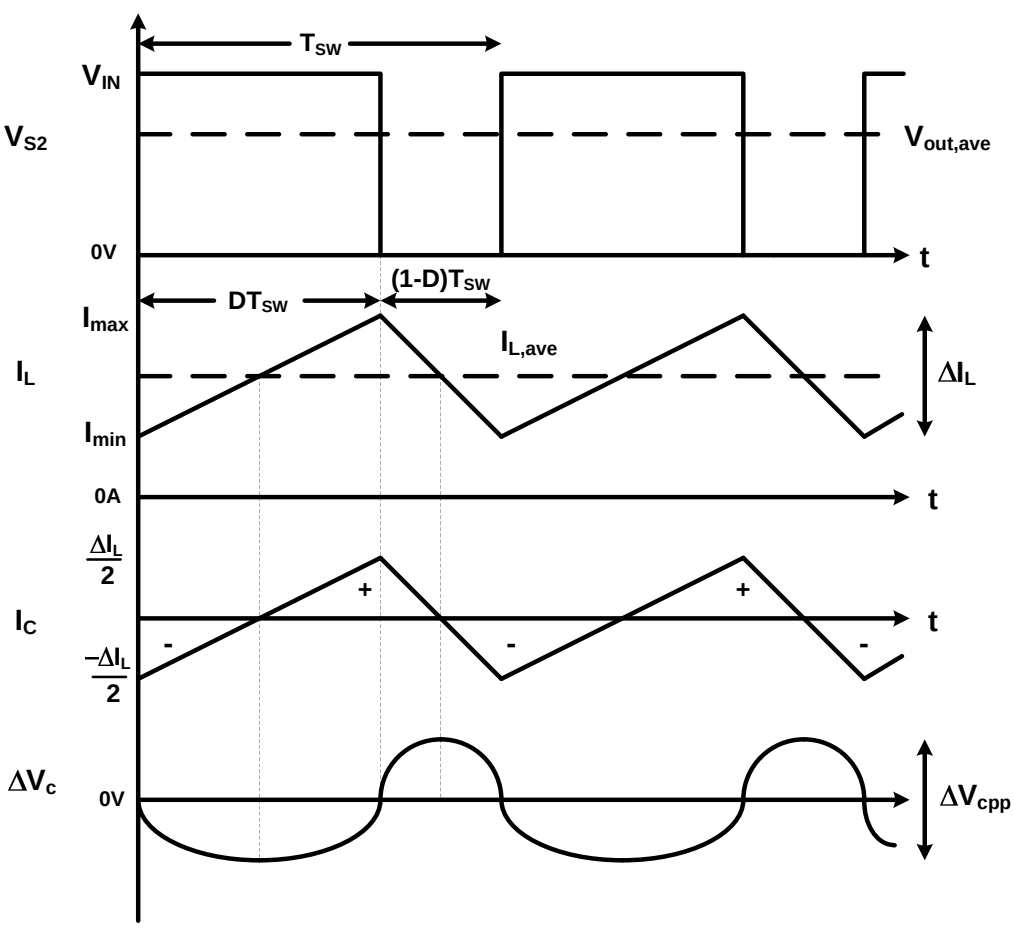
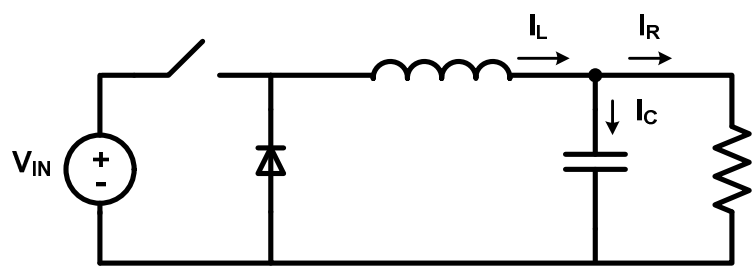


Figure 1.8: Steady-State Buck Chopper Waveforms Assuming CCM

To correctly arrive at the capacitor current waveshape, first recall that the capacitor current constitutive relationship is given by

$$I_C = C\frac{dV_C}{dt} \tag{1.16}$$

If the capacitor current has an average value, then $V_{C,ave}$ is not constant. Thus in the steady state, it is necessary that $I_{C,ave} = 0$ (think of this as if the average capacitor current was positive, then the capacitor would on average be charging to a higher voltage value). Furthermore, by applying KCL at the output circuit node, it follows that



$$I_{L,ave} = I_{C,ave} + I_{R,ave} \tag{1.17}$$

Therefore

$$I_{L,ave} = I_{R,ave} = \frac{V_{out,ave}}{R} \tag{1.18}$$

We can then determine expressions for the maximum and minimum inductor current values since we established (from 1.11 where that expression gives a negative value so we flip the sign) that

$$\Delta I_L = \frac{V_{out,ave}}{L}(1-D)T_{SW} = \frac{V_{out,ave}(1-D)}{Lf_{SW}} \tag{1.19}$$

Thus

$$I_{\max} = I_{L,ave} + \frac{\Delta I_L}{2} \tag{1.20}$$

$$I_{\min} = I_{L,ave} - \frac{\Delta I_L}{2} \tag{1.21}$$

What does this all mean? Well, the average inductor current directly depends on the applied load resistance and the desired output average voltage (as set by the duty cycle).

A small value of R corresponds to a large value of average current and vice versa. The inductor ripple current <u>does not depend on the load resistance</u>, thus once the switching frequency is set, the ripple current is set as shown in Figure 1.9. We see something interesting in Figure 1.9, as the load power drops ($I_{L,ave} \downarrow$ and $R \uparrow$) the inductor current will eventually hit zero while the diode is conducting, turning the diode off (before the switch S_1 turns ON). This will transition the circuit into the Discontinuous Conduction Mode (DCM) and the nice steady-state linear relationship $V_{out,ave} = DV_{IN}$ no longer holds. A typical DCM inductor current waveform is shown in Figure 1.10. Fortunately, a buck chopper typically employs feedback control to compensate for component parasitics, changes in load, and changes in the input so it will *automatically* find the proper D to achieve the desired output voltage.

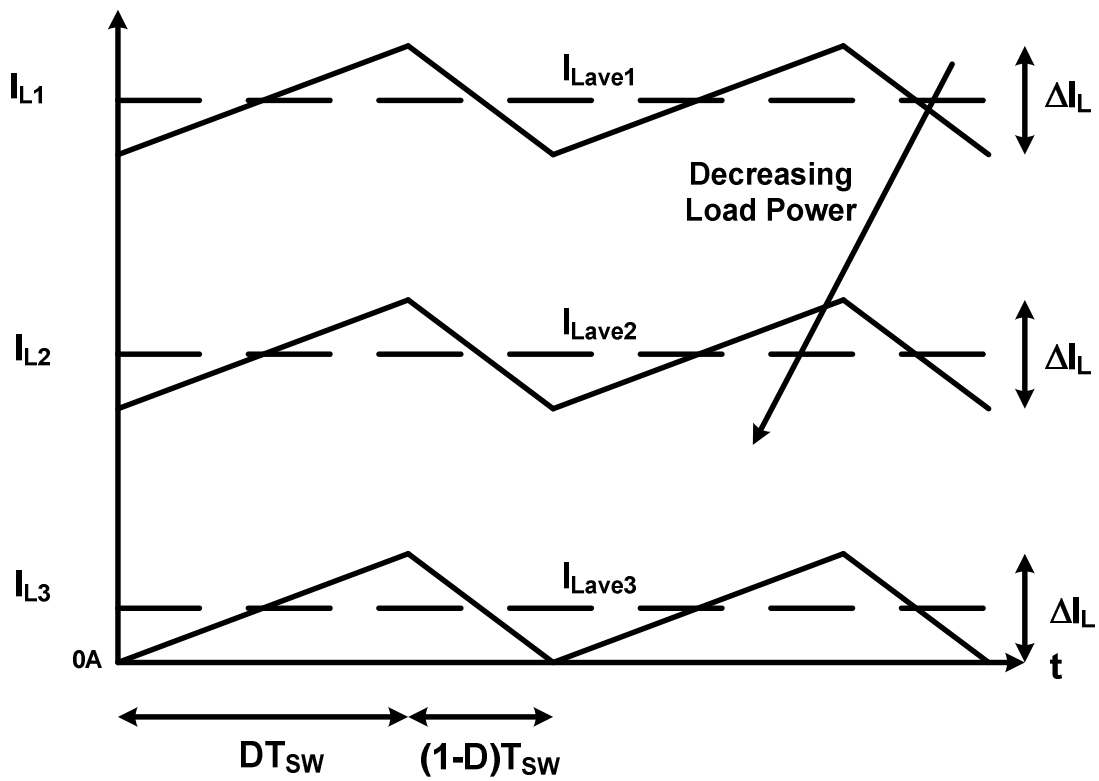


Figure 1.9: Inductor Currents in CCM for Varying Amounts of Load Resistance

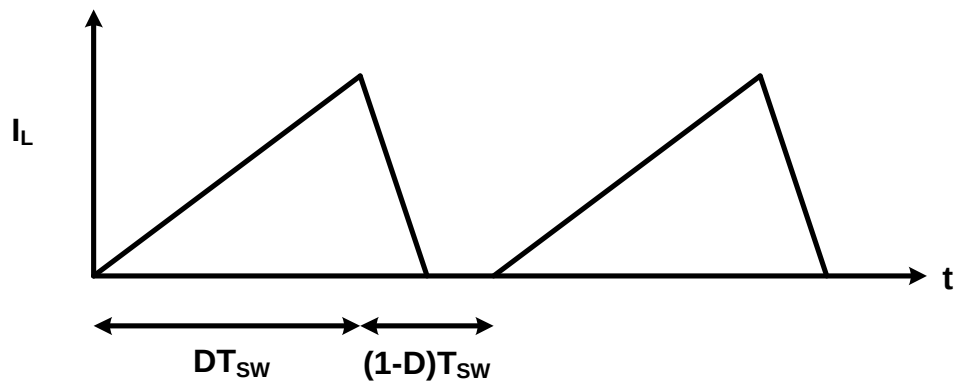


Figure 1.10: Inductor Current in DCM

The transition point between CCM and DCM is a useful point to derive. It occurs when the minimum value of the inductor current just hits zero or $I_{\min} = I_{L,ave} - \frac{\Delta I_L}{2} = 0$. If we substitute (1.18) and (1.19), we come up with

$$\frac{V_{out,ave}}{R} - \frac{V_{out,ave}(1-D)}{2 f_{SW} L_{crit}} = 0 \tag{1.22}$$

We can solve this for the *critical inductance* (L_{crit}) value when the load resistance is the largest value that we would like to maintain the converter in CCM and we find that

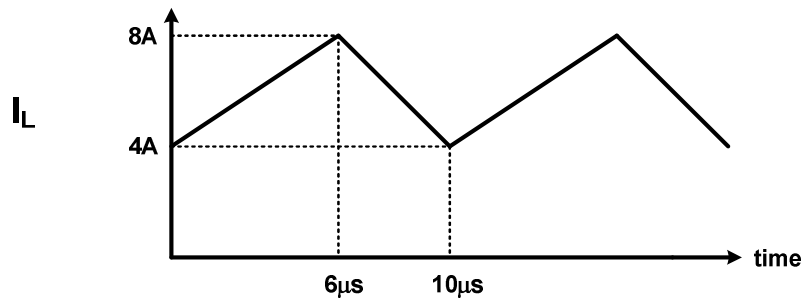
$$L_{crit} = \frac{(1-D)R_{big}}{2 f_{SW}} \tag{1.23}$$

Equation (1.23) offers one approach to designing the inductor value for the buck chopper. The resistance R_{big} is given by

$$R_{big} = \frac{V_{out,ave}^2}{P_{crit}} \tag{1.24}$$

Where P_{crit} is the output power level where you want your buck chopper to transition into DCM. A smaller P_{crit} will lead to a larger L and a smaller inductor ripple. A larger value of inductance will mean a physically larger inductor with more losses, which sounds unattractive. But if one shoots for a larger P_{crit} so that L is smaller and the ripple current is bigger, what is the downside? Well, we will find that this requires a larger capacitor with more ripple current capability which sounds like there is an engineering tradeoff afoot! Unfortunately equations (1.23) and (1.24) really do not illustrate this tradeoff so we will have to figure out something better.

Example 1.3: Given an ideal buck chopper with $V_{in} = 20V$ and the following inductor current waveform



Determine (a) the duty cycle and switching frequency, (b) the average output voltage, (c) the circuit inductance, (d) the load resistance for the operating point pictured, and (e) the load resistance that transitions the converter to discontinuous conduction mode.

a. The duty cycle is given by the ratio of ON time (ramp-up time) to switching period. The switching frequency is the inverse of the switching period so

$$D = \frac{6\mu s}{10\mu s} = 0.6 \qquad\qquad f_{sw} = \frac{1}{10\mu s} = 100kHz$$

b. The ideal input/output relationship for a buck chopper is $V_{out,ave} = DV_{in}$ thus

$$V_{out,ave} = 0.6 \times 20V = 12V$$

c. We can use either (1.8) or (1.11). Rearranging (1.8) to solve for the inductance yields

$$L = \left(\frac{V_{in} - V_{out,ave}}{\Delta I_{L,ON}}\right) DT_{sw} = \left(\frac{20V - 12V}{8A - 4A}\right) 0.6 \times 10\mu s = 12\mu H$$

d. The average value of the inductor current is in the center of the waveform, so it follows that $I_{L,ave} = (4A + 8A)/2 = 6A$. Since the average capacitor current must be zero, *the average load current must equal the average inductor current* and

$$R = \frac{V_{out,ave}}{I_{out,ave}} = \frac{12V}{6A} = 2\Omega$$

e. The transition to DCM occurs when $I_{L,ave} = \frac{\Delta I_L}{2} = \frac{4A}{2} = 2A$. This occurs when the output resistance equals $R_{big} = 12V / 2A = 6\Omega$

Example 1.4: Consider that we want to design a buck chopper that will step 24V down to 12V with a maximum output power of 100W. For a switching frequency of 40kHz, investigate the change in design if (a) $P_{crit} = 10W$ or (b) $P_{crit} = 20W$

a. First, we evaluate the required duty cycle $D = V_{out,ave} / V_{in} = 12V / 24V = 0.5$, Next we calculate the load resistance corresponding to the critical power

$$R_{big} = \frac{(12V)^2}{10W} = 14.4\Omega$$

The critical inductance is then given by (1.23)

$$L_{crit} = \frac{(1-0.5)\times 14.4\Omega}{2\times 40,000Hz} = 90\mu H$$

The corresponding inductor ripple current is then found via (1.19) to be

$$\Delta I_L = \frac{12V\times(1-0.5)}{90\mu H\times 40kHz} = 1.67A$$

With proper design of the output capacitor, most of this ripple current will then flow through the capacitor (so the output current ripple is small)

b. Repeating the design for a higher critical power yields

$$R_{big} = \frac{(12V)^2}{20W} = 7.2\Omega$$

The critical inductance becomes

$$L_{crit} = \frac{(1-0.5)\times 7.2\Omega}{2\times 40,000Hz} = 45\mu H$$

which results in a new required inductor ripple current

$$\Delta I_L = \frac{12V\times(1-0.5)}{45\mu H\times 40kHz} = 3.33A$$

Thus, we see a tradeoff in specifying a higher value of critical power. The required inductance is smaller (so it will be physically smaller) but the ripple current must be larger (which will result in a larger required capacitance).

Let's next consider focusing in on the steady-state output voltage ripple ΔV_C shown in Figure 1.8. Note that with the output voltage ripple assumed to be much smaller than its average value, most of the inductor current ripple must go through the capacitor. Because $I_C = C\dfrac{dV_C}{dt}$, when the capacitor current is positive, the capacitor voltage is building and when the capacitor current is negative, the capacitor voltage is decreasing. Since the capacitor current must have zero average value for the circuit to be in the steady state, this implies that the area above zero must be the same as the area below zero. Since the positive and negative capacitor current peaks have the same magnitude, we can deduce that the capacitor current is positive for half of the switching period and negative for the other half. By integrating the capacitor governing relationship we get that the capacitor charge is equal to

$$\Delta Q_C = C\Delta V_C \tag{1.25}$$

The change in charge while the current is positive is found by calculating the area under the triangle whereas the change in voltage will be ΔV_{Cpp} as shown in Figure 1.8.

$$\Delta Q_C = \frac{1}{2}(base)(height) = \frac{1}{2}\left(\frac{T_{SW}}{2}\right)\left(\frac{\Delta I_L}{2}\right) = C\Delta V_{Cpp} \tag{1.26}$$

If we solve for the capacitance and replace the switching period by one over the switching frequency, we get

$$C_{\min} = \frac{\Delta I_L}{8 f_{SW}\Delta V_{Cpp}} \tag{1.27}$$

This tells us that the smaller the ripple, the bigger the capacitance (which makes intuitive sense). Like (1.23), equation (1.27) is encouraging in that both the critical inductance and the minimum capacitance are inversely related to the switching frequency which is what we deduced from our original filter analysis (a higher switching frequency can allow us to have a bigger ω_o, implying smaller values for L and C). Unfortunately (1.27) is not the end of the story because by its name $C_{\min}$ implies that it is the minimum permissible for the value of ripple, but how much higher should we go and why? One might quickly observe that more capacitance means more volume and more cost so don't go any higher. This ignores the fact that we also want our buck chopper to behave well under transient conditions (changes in load or input) and we will find that the capacitance will intimately impact this dynamic. Also, we will find that a key capacitor specification is the RMS ripple current through it and that bigger capacitors have more ripple current capability.

<u>Example 1.5</u>: Given the buck chopper design from Example 1.4a (where $V_{out,ave} = 12V$), if we impose a maximum output voltage ripple of 1% of the average value ($\Delta V_{Cpp} \leq 0.01 \times 12V = 120mV$), determine the required capacitance.

From (1.27), we get

$$C_{\min} = \frac{1.67A}{8 \times 40kHz \times 0.12V} = 61\mu F$$

This is not a standard value of capacitance, so we would scale up to the next largest standard value ($68\mu F$). However, the story does not end here since it will be very important that this capacitor be able to handle the expected 1.67A peak-to-peak ripple current from the inductor. More on this in the next chapter.

OK, so to address the transient capability link to C, let's consider a worst case scenario. We are operating at maximum load, the inductor current is at its peak value, and we disconnect the load resistance. The situation is illustrated in Figure 1.11. What happens? When the load becomes disconnected (or R gets very big), the inductor current cannot change instantaneously and so all of it will flow through the capacitor, including its average value. This will tend to increase the capacitor voltage. As the voltage builds beyond $V_{out,ave}$, the control algorithm will reduce D and in this case most likely drive it to zero (it does not benefit the system at this point to close the switch S_1 since this only dumps more energy into the inductor; energy which will need to be dissipated somewhere). Thus with S_1 open, the diode conducts until I_L drops all the way to zero. We can estimate the change in capacitor voltage by performing an energy balance between the two conditions.

$$E_{before,dropload} = E_{after,dropload} \tag{1.28}$$

Substituting gives

$$\frac{1}{2}CV_{out,ave}^2 + \frac{1}{2}LI_{pk}^2 = \frac{1}{2}C\left(V_{out,ave} + \Delta V_{trans}\right)^2 \tag{1.29}$$

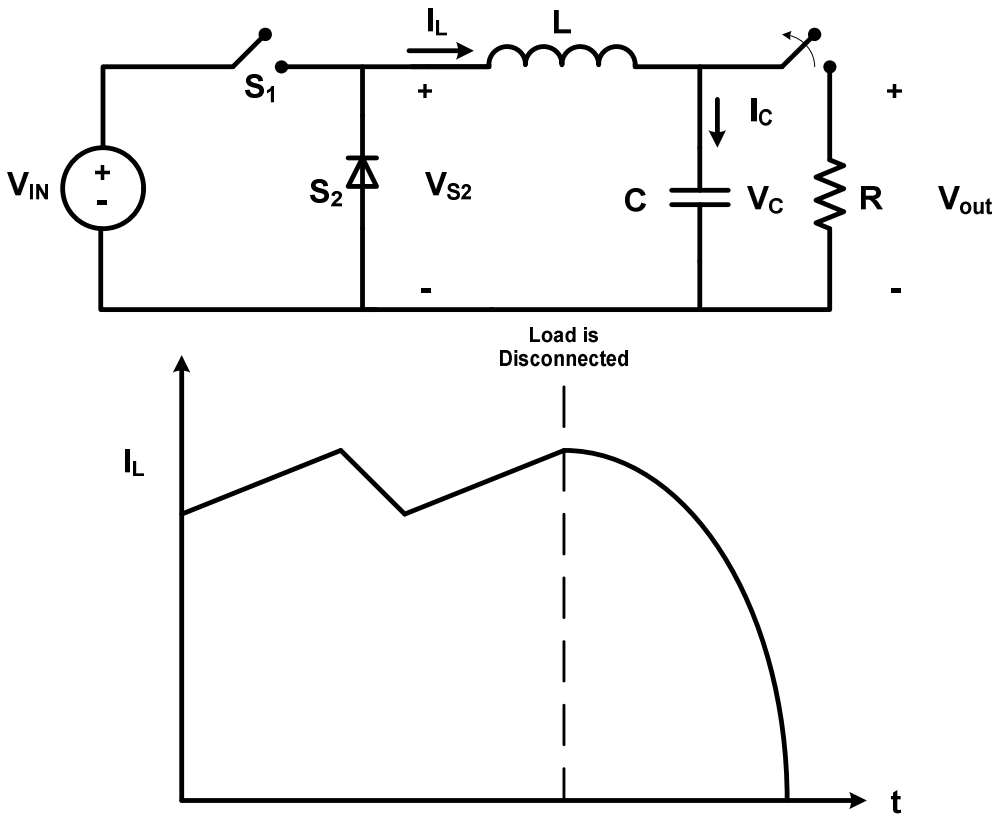


Figure 1.11: Drop Load Scenario

Solving for C in (1.29) yields

$$C = \frac{LI_{pk}^2}{\left(V_{out,ave} + \Delta V_{trans}\right)^2 - V_{out,ave}^2} = \frac{L\left(I_{L,ave,\max} + \frac{\Delta I_L}{2}\right)^2}{\left(V_{out,ave} + \Delta V_{trans}\right)^2 - V_{out,ave}^2} \tag{1.30}$$

Yikes what is (1.30) saying? Well ΔV_{trans} is approximately how much above $V_{out,ave}$ that we are willing to allow the output voltage to rise if we go from 100% power out to 0% power out. Obviously choosing ΔV_{trans} equal to zero yields infinite capacitance and an impractical solution. If we choose $\Delta V_{trans} = 0.4142 V_{out,ave}$ (essentially a 41% overshoot), the choice of capacitance will balance the energy between the inductor and the capacitor, and it is an interesting compromise value that is typically much larger than the value found in (1.27). A more thorough tradeoff analysis requires a detailed dynamic simulation, including the feedback control, which is beyond our current mission!

Example 1.6: Considering examples 1.4a and 1.5, let's consider that we wish to assess how much the capacitor value must change to balance the peak energies in the inductor and capacitor.

The peak inductor current is found using (1.20)

$$I_{L,\max} = I_{L,ave} + \frac{\Delta I_L}{2} = \frac{100W}{12V} + \frac{1.67A}{2} = 9.17A$$

The energy in the inductor is then found from

$$E_{L,\max} = \frac{1}{2} L I_{L,\max}^2 = \frac{1}{2} \times 90\mu H \times (9.17A)^2 = 3.784mJ$$

If we set this value to the maximum energy in the capacitor (ignoring the small value of ripple)

$$E_{C,\max} = \frac{1}{2} C V_{out,ave}^2 = \frac{1}{2} \times C \times (12V)^2 = 3.784mJ$$

We get a required capacitance of $52.6\mu F$ (or less than the value required for assuring our steady-state ripple, $61\mu F$). Thus in this case, the steady-state requirement is more restrictive than the transient requirement. The ability to handle the inductor ripple current will ultimately drive the final selection of capacitance.

OK, we have argued that (1.23) (the equation for L_{crit}) and (1.24) (the equation for R_{big}) are not particularly insightful engineering formulas to determine inductance and have now found a formula for capacitance that depends on L, so matters are *not* improving. Let's make an argument based on the following observation: the ripple current does not depend on the load resistance but it does depend on L. So let's propose that the ratio of the ripple current to the maximum average load current might make for an interesting parameter to consider.

$$r = \frac{\Delta I_L}{I_{L,ave,\max}} \tag{1.31}$$

The inductor ripple current is related to the inductance via (1.19) so we can "massage" this expression to place it in terms of the *ripple ratio r*

$$L = \frac{V_{out,ave}(1-D)}{\Delta I_L f_{SW}} \times \frac{I_{L,ave,\max}}{I_{L,ave,\max}} = \frac{V_{out,ave}(1-D)}{r f_{SW} I_{L,ave,\max}} \tag{1.32}$$

The inductor peak energy will relate to the volume of inductor required. This can be quantified by

$$E_{L,pk} = \frac{1}{2} L I_{L,pk}^2 = \frac{1}{2} \frac{V_{out,ave}(1-D)}{r f_{SW} I_{L,ave,\max}} \left(I_{L,ave,\max} + \frac{\Delta I_L}{2} \right)^2 \tag{1.33}$$

We can rewrite this in terms of the ripple ratio 'r' as

$$E_{L,pk} = \frac{1}{2} \frac{V_{out,ave}(1-D)}{r f_{SW} I_{L,ave,\max}} I_{L,ave,\max}^2 \left(1+\frac{r}{2}\right)^2 = \frac{1}{2} \frac{V_{out,ave}(1-D)}{f_{SW}} I_{L,ave,\max} \frac{\left(1+\frac{r}{2}\right)^2}{r} \tag{1.34}$$

This expression tells us how the energy in the inductor will vary with a given value of ripple ratio. The other variables in (1.34) are generally specified (output voltage and maximum load) while the switching frequency will need to be selected based on other factors. If we plot the *normalized* version of (1.34) for a range of $0 < r \le 2$

$$E_{L,pk,norm} = \frac{\left(1+\frac{r}{2}\right)^2}{r} \tag{1.35}$$

we get the plot shown in Figure 1.12. An r = 2 implies that the rated load condition is at the boundary of DCM. Note that below r = 0.2, the required inductor energy (think size of inductor) increases very quickly. If r is small, the ripple current is small which necessitates a large inductance and therefore a large peak energy capability. Beyond r = 0.6, the normalized energy decreases rather slowly, so we are not gaining much more advantage. We will next see that there is an added disadvantage to designing with a larger value of 'r'.

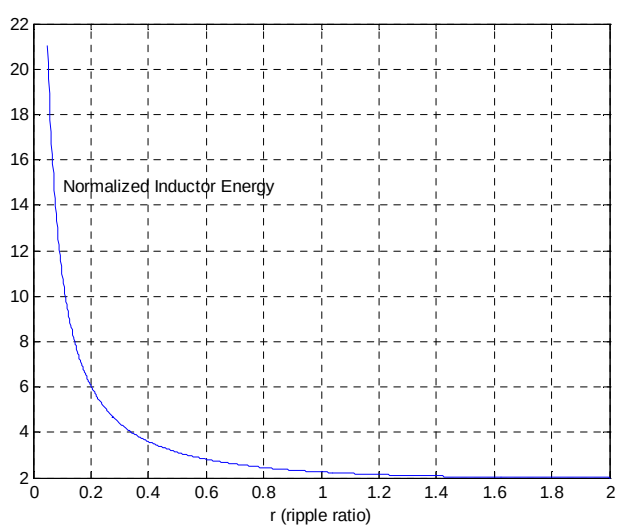


Figure 1.12: Plot of Normalized Inductor Energy versus the Ripple Current Ratio

Why are larger values of 'r' unattractive? Let's start with the capacitor current and determine its RMS value. If we consider the signal I_C shown in Figure 1.8, we must find the RMS value of a symmetrical triangle wave. Omitting the details, this value equals its peak value divided by the square root of three, or

$$I_{C,rms} = \frac{I_{pk}}{\sqrt{3}} = \frac{\Delta I_L / 2}{\sqrt{3}} = \frac{\Delta I_L}{\sqrt{12}} \tag{1.36}$$

If we would prefer to write this in terms of the ripple ratio $r = \frac{\Delta I_L}{I_{L,ave,\max}}$, then we get

$$I_{C,rms} = \frac{I_{L,ave,\max}}{\sqrt{12}} r \tag{1.37}$$

This implies that we suffer a penalty in selecting r too large – a larger capacitor ripple requirement which will mean more capacitance or more capacitors.

Thus if r < 0.2, the ripple is small, so the inductance is large and since for transient concerns we try to match the capacitor energy to the inductor energy, this implies a large value of capacitance. For r > 0.6, the inductor energy goes down more slowly and the capacitor ripple current requirement linearly increases, implying that more capacitance is required. Therefore we postulate that an "attractive" range for the ripple ratio is $0.2 \le r \le 0.6$. This corresponds to a critical power range of $0.1P_{rat} \le P_{crit} \le 0.3P_{rat}$. By investigating this range across the design space (the set of reasonable parameter values and components) and evaluating a figure of merit like efficiency, size, or cost, we can then determine a "best" choice for 'r.' MATLAB or EXCEL are excellent programs that can facilitate this "spread sheet" approach to design!

Our analysis thus far has assumed ideal components, switches that have zero voltage drops. If V_{IN} and V_{out} are above 50V, this is not a bad assumption. But what if the input and output voltage are less than 12V? Then a 0.5V-1V switch drop will start to influence the calculations. As a result, let's incorporate these voltage drops in our analysis and reformulate our expression for L_{crit}. The analysis proceeds as before using the circuits shown in Figure 1.13.

The change in inductor current while the switch is closed (Figure 1.13a) is found to be

$$\Delta I_{L,ON} = \frac{V_{IN} - V_{SW} - V_{out,ave}}{L} DT_{SW} \tag{1.38}$$

where V_{SW} is the assumed constant voltage drop across the switch. Similarly using Figure 1.13b for when the diode is conducting, we can find the change in inductor current to be

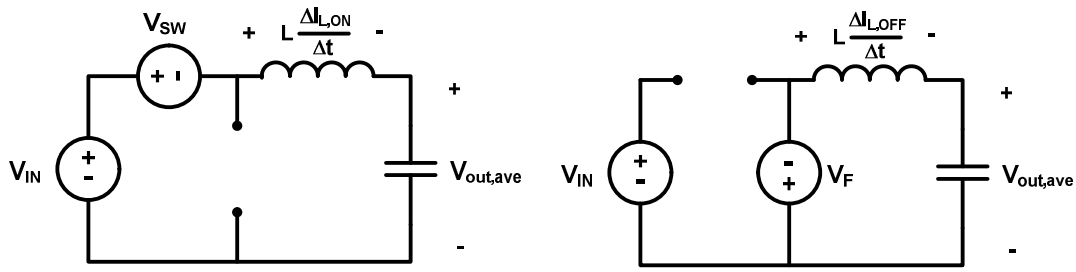
$$\Delta I_{L,OFF} = \frac{-V_F - V_{out,ave}}{L}(1-D)T_{SW} \tag{1.39}$$

where V_F is the assumed voltage drop across the diode. In the steady state we can assert that

$$\Delta I_{L,ON} + \Delta I_{L,OFF} = 0 \tag{1.40}$$

which upon substituting and simplifying yields

$$D = \frac{V_{out,ave} + V_F}{V_{IN} - V_{SW} + V_F} \tag{1.41}$$



(a) (b)

Figure 1.13: Buck Chopper Analysis with Switch and Diode Replaced by Voltage Drops: (a) Switch Closed, Diode OFF; (b) Switch Open, Diode ON

Since the change in current shown in Equation (1.39) is negative, we can flip the sign and solve for the inductance as

$$L_{crit} = \frac{(V_{out,ave} + V_F)(1-D)}{\Delta I_L f_{SW}} \tag{1.42}$$

or finally in terms of the ripple ratio $r = \dfrac{\Delta I_L}{I_{L,ave,\max}}$

$$L_{crit} = \frac{(V_{out,ave} + V_F)(1-D)}{r f_{SW} I_{L,ave,\max}} \tag{1.43}$$

Thus upon establishing estimates of the average switch and diode voltage drops, you can use (1.41) and (1.43) to determine the critical inductance. As can be the case, if the input voltage varies, then you will want to determine the worst case (largest) required inductance. From (1.43), the inductance gets bigger when ‘D’ gets smaller. Therefore from (1.41), ‘D’ gets smaller when the input is its largest value.

Example 1.7: Consider that we want to re-design the buck chopper from Example 1.4 that steps 24V down to 12V with a maximum output power of 100W with a switching frequency of 40kHz and $P_{crit} = 10W$ (r = 0.2). This time let's assume that we have a switch voltage drop of $V_{SW} = 1.8V$ and a diode drop of $V_F = 1.2V$.

Equation (1.41) gives us an estimate of the new required duty cycle

$$D = \frac{12V + 1.2}{24V - 1.8V + 1.2V} = 0.564$$

which is slightly larger than the "ideal" analysis value of 0.5. We can then evaluate the critical inductance using (1.43)

$$L_{crit} = \frac{(12V + 1.2V)(1 - 0.564)}{0.2 \times 40,000 \times \frac{100W}{12V}} = 86.3\mu H$$

Here, we see that the inductance did not change appreciably (decreasing from the ideal value of $90\mu H$). With the ripple ratio set to $r = 0.2 = \frac{\Delta I_L}{I_{L,ave,\max}}$. The inductor ripple current must equal

$$\Delta I_L = 0.2 \times I_{L,ave,\max} = 0.2 \times \frac{100W}{12V} = 1.67A$$

as we had before. Thus, the sizing of the capacitor as performed in Example 1.5 would be unchanged and the result in Example 1.6 would be slightly smaller since the value of L is slightly smaller.

Example 1.8: Let's explore how a design proceeds when the input voltage can change. Let's assume that we wish to design a DC-DC converter that will step a 12V battery down to 5V. The terminal voltage of the battery can vary between 11V and 14V based on the state of charge. The rated output power is specified as 15W. We are asked to use a switching frequency of 20kHz and a ripple ratio of 0.2 $\left(P_{crit} = P_{rat}/10 = 15W/10 = 1.5W\right)$. The output ripple voltage should be no more than 1% of the average output voltage. Establish values for the buck chopper inductance and capacitance. Assume that the selected switch and diode have voltage drops of 0.3V and 0.5V, respectively.

OK, so the issue is which value of V_{in} do we use in (1.41) to estimate the duty cycle. To convince ourselves, let's work through the calculations using both. Starting with the minimum input voltage we get

$$D_1 = \frac{5V + 0.5V}{11V - 0.3V + 0.5V} = 0.491$$

The corresponding value of critical inductance is then found from (1.43)

$$L_{crit,1} = \frac{(5V + 0.5)(1 - 0.491)}{0.2 \times 20,000 \times \frac{15W}{5V}} = 233\mu H$$

If we repeat for the larger value of input voltage, the new duty cycle is

$$D_2 = \frac{5V + 0.5V}{14V - 0.3V + 0.5V} = 0.387$$

And the new critical inductance is

$$L_{crit,2} = \frac{(5V + 0.5)(1 - 0.387)}{0.2 \times 20,000 \times \frac{15W}{5V}} = 281\mu H$$

So clearly, the worst-case design must occur at the higher input voltage which presents us with a larger required inductance. The ripple current is fixed by the ripple ratio (or the critical power level) $\Delta I_L = 0.2 \times I_{L,ave,\max} = 0.2 \times (15W / 5V) = 0.6A$. Thus we can then estimate the minimum capacitance for steady-state ripple from (1.27)

$$C_{\min} = \frac{\Delta I_L}{8 f_{sw} \Delta V_{Cpp}} = \frac{0.6A}{8 \times 20kHz \times 0.01(5V)} = 75\mu F$$

If we contrast this with equating the energies in the capacitor and inductor at rated power, we get

$$C = \frac{L_{crit} I_{L,pk}^2}{V_{out,ave}^2} = \frac{281\mu H \times (3A + 0.6A)^2}{(5V)^2} = 146\mu F$$

So for transient reasons, we might like to choose a value closer to $150\mu F$. Finally though, we will learn in the next chapter that the capacitor must be able to handle the inductor ripple current which is specified via the rms value found in (1.36)

$$I_{C,rms} = \frac{\Delta I_L}{\sqrt{12}} = \frac{0.6A}{\sqrt{12}} = 173mA$$