## 4.0 Buck Converter Controllable Switch

The switch $S_1$ in the buck chopper pictured in Figure 4.1 must be "fully-controllable." This means that we must be able to both turn it ON and turn it OFF with a control signal versus relying on circuit signals changing to initiate device turn on or turn off. In the power arena, there are four prominent controllable switches that are available: the bipolar junction transistor (BJT), the metal-oxide semiconductor field-effect transistor (MOSFET), the insulated-gate bipolar transistor (IGBT), and the gate-turn-off thyristor (GTO). The circuit symbol for each is pictured in Figure 4.2.

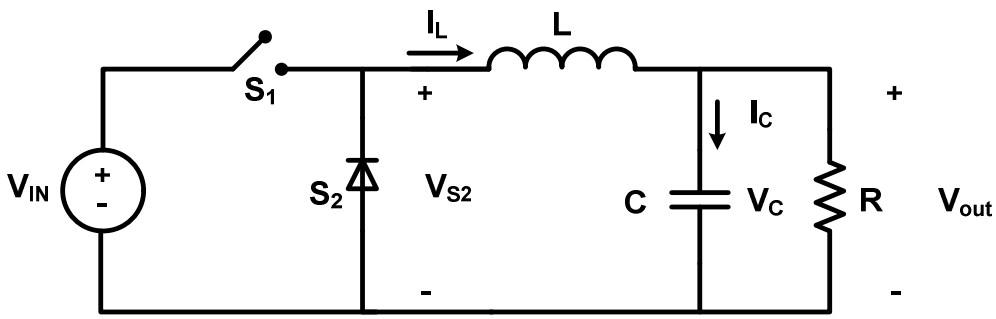
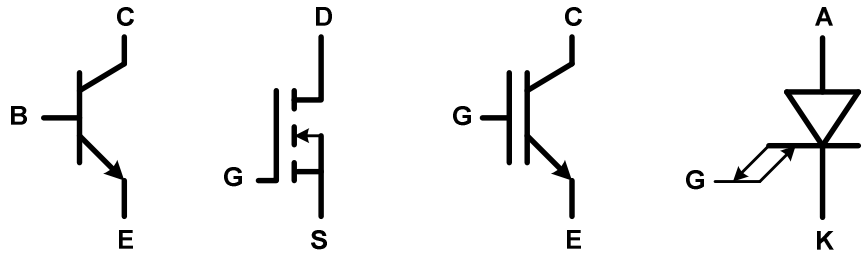



Figure 4.1: Buck Converter Topology

A comprehensive discussion of each switch type is beyond the scope of this document. In its place, we will briefly describe the key attributes of an electronic switch and focus in on the MOSFET which is most commonly found in low-power power supplies. If we review the buck converter operation, we would like switch $S_1$ to (1) have zero volts across it when it is conducting, (2) conduct as much current as necessary, (3) have zero current through it when it is OFF, (4) transition between ON/OFF states without loss, and (5) be able to operate at very high switching frequencies, where the circuit inductor and capacitor can be made much smaller.




(a) (b) (c) (d)

Figure 4.2: Controllable Switches: (a) BJT; (b) MOSFET; (c) IGBT; (d) GTO

A "real" semiconductor switch cannot fully achieve these "ideal" characteristics. Therefore, we modify the requirements to match the realities of what the various technologies can offer. An electronic switch must be able to:

1. Withstand the voltage across it when it is OFF (blocking)
2. Conduct current without excessive losses when it is ON
3. Turn ON and OFF quickly to minimize switching losses
4. Interface conveniently to control signals
5. Safely dissipate its power losses using conductive/convective means

In terms of making a transistor look like a switch, we are probably most familiar with the BJT. If we apply a large enough base current, we drive the transistor into saturation thereby making the collector-emitter voltage small. Unfortunately this large continuously-applied base current complicates the control interface and further, since the BJT uses both electron and hole conduction, its switching speed is relatively slow due to the high carrier lifetime of the holes. As a consequence, the BJT has been pretty much surpassed in performance by both the MOSFET and IGBT. For high switching frequency and low power applications, the MOSFET has superior performance. For higher voltage and current applications, the IGBT has superior performance. The GTO dominates the controllable-switch arena for very high power applications. Some representative switch ratings are listed in Table 4.1 along with the manufacturer. Since we have limited time to dedicate to switch technology and since the MOSFET is ubiquitous in power supply applications, we will focus on it.

Table 4.1: Controllable Switch Technology Bounds

| Device | Vendor | Voltage | Current |
|---|---|---|---|
| MOSFET | STMicroelectronics | 1500V | 4A |
| | Microsemi-PPG | 1200V | 34A |
| | IXYS | 600V | 85A |
| | Semikron | 200V | 500A |
| | IXYS | 100V | 690A |
| IGBT | Eupec | 6500V | 600A |
| | Eupec | 3300V | 1200A |
| | Eupec | 1700V | 3600A |
| GTO | Mitsubishi | 6000V | 3100Arms |

The MOSFET (FET for short) is a *unipolar* conducting device meaning that there are no minority carriers, only electrons flow. FETs can be N-channel (NFET or HEXFET) or P-channel (PFET) devices, though we will focus on the N-channel variety for performance reasons. When a gate-to-source voltage greater than the threshold voltage ($V_{GS,TH}$) is applied, a channel is created between the drain and source which accommodates the electron flow as shown in Figure 4.3. The resistance of this channel decreases as the gate-to-source voltage is further increased and the FET transitions from the “linear” mode into “saturation.” For switch applications where we desire to operate in saturation, the channel resistance parameter is referred to as the on-resistance $R_{DS,ON}$ and as $V_{GS}$ increases, it decreases up until $V_{GS}$ is 8 to 12V. Due to the thin gate oxide, the gate voltage is typically limited to about 20V before the device is damaged.

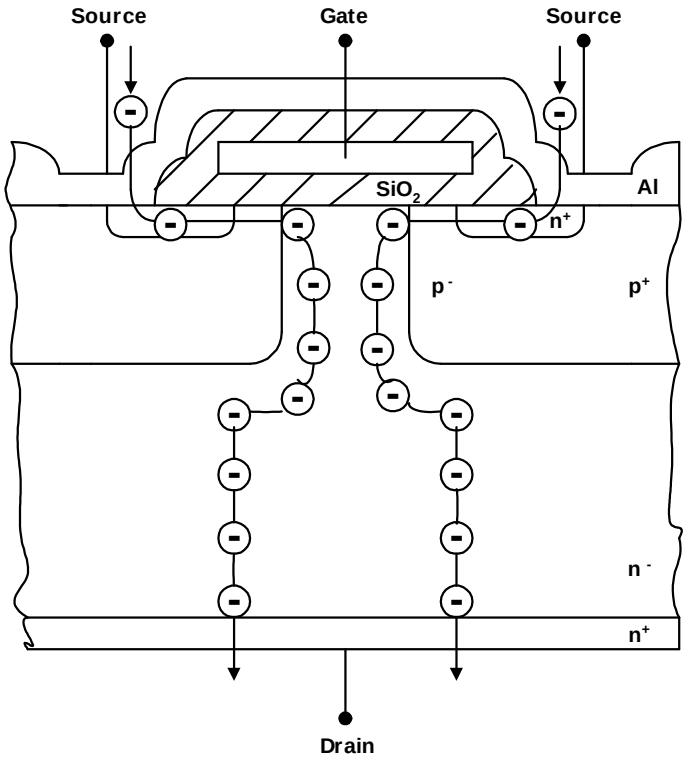



Figure 4.3: N-Channel MOSFET Physical Structure Showing Electron Flow

A finite time is required to transition the FET from cutoff to saturation as the intrinsic device capacitances are charged and $V_{GS}$ builds. Let's next go through and describe the turn-on and turn-off transitions. We will consider a "clamped inductive" situation where the FET is attached to an inductor so the inductor current does not change much during the switching transient. This arrangement is illustrated in Figure 4.4 where the inductor is modeled by a current source of value $I_{D,ON}$. Thus when the FET is OFF, the current $I_{D,ON}$ flows through the ideal diode in parallel and the voltage across the FET is equal to $V_{DS,OFF}$. The parameters $V_{DR}$ and $R_{DR}$ represent the Thevenin equivalent of a *gate driver* (that we will talk about in a bit) and $R_{Gext}$ is external resistance that we will place in between the driver and gate to limit the gate current and control the switching speed.

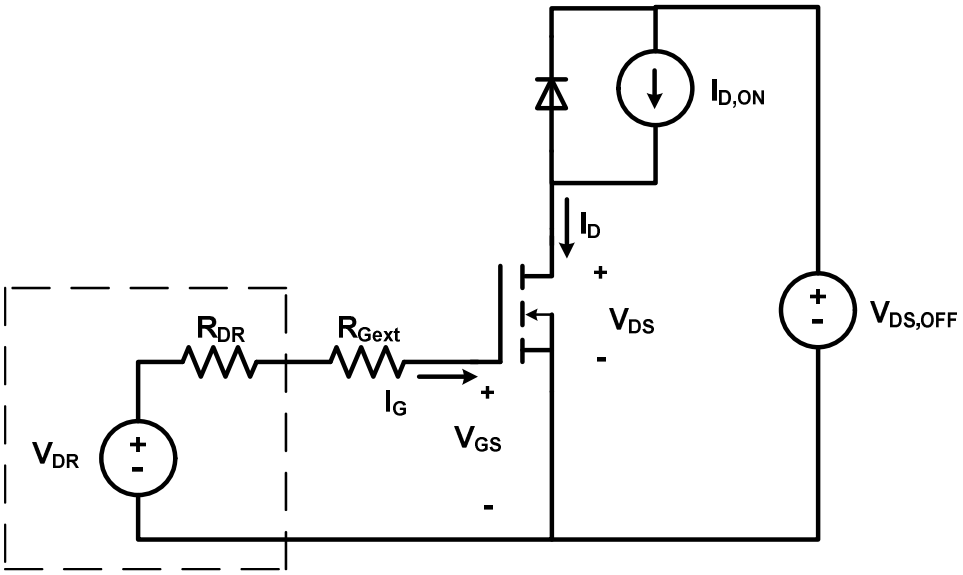



Figure 4.4: Clamped-Inductive Load to Illustrate FET Switching

Figure 4.5 shows the identical circuit but this time the parasitic capacitances $C_{GS}$, $C_{GD}$, and $C_{DS}$ are illustrated. Also, we see that the semiconductor processing also creates what is termed a "body diode" from the source to the drain. This internal diode BD is sometimes used in circuits that require a "free-wheeling" diode to carry current from source to drain. This diode is not used in the basic buck topology considered. The idealized turn-on transient is shown in Figure 4.6. We say "idealized" since the actual voltage and current trajectories will be more nonlinear and can depend on other parasitic effects such as package, source and connection inductances.

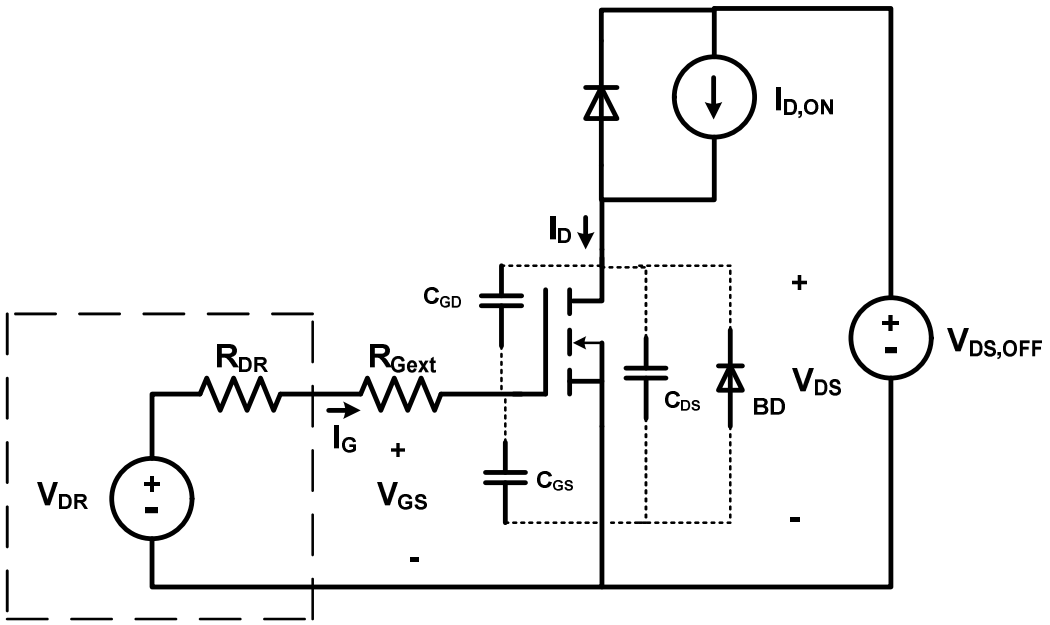



Figure 4.5: FET Circuit with Parasitic Capacitances and Body Diode

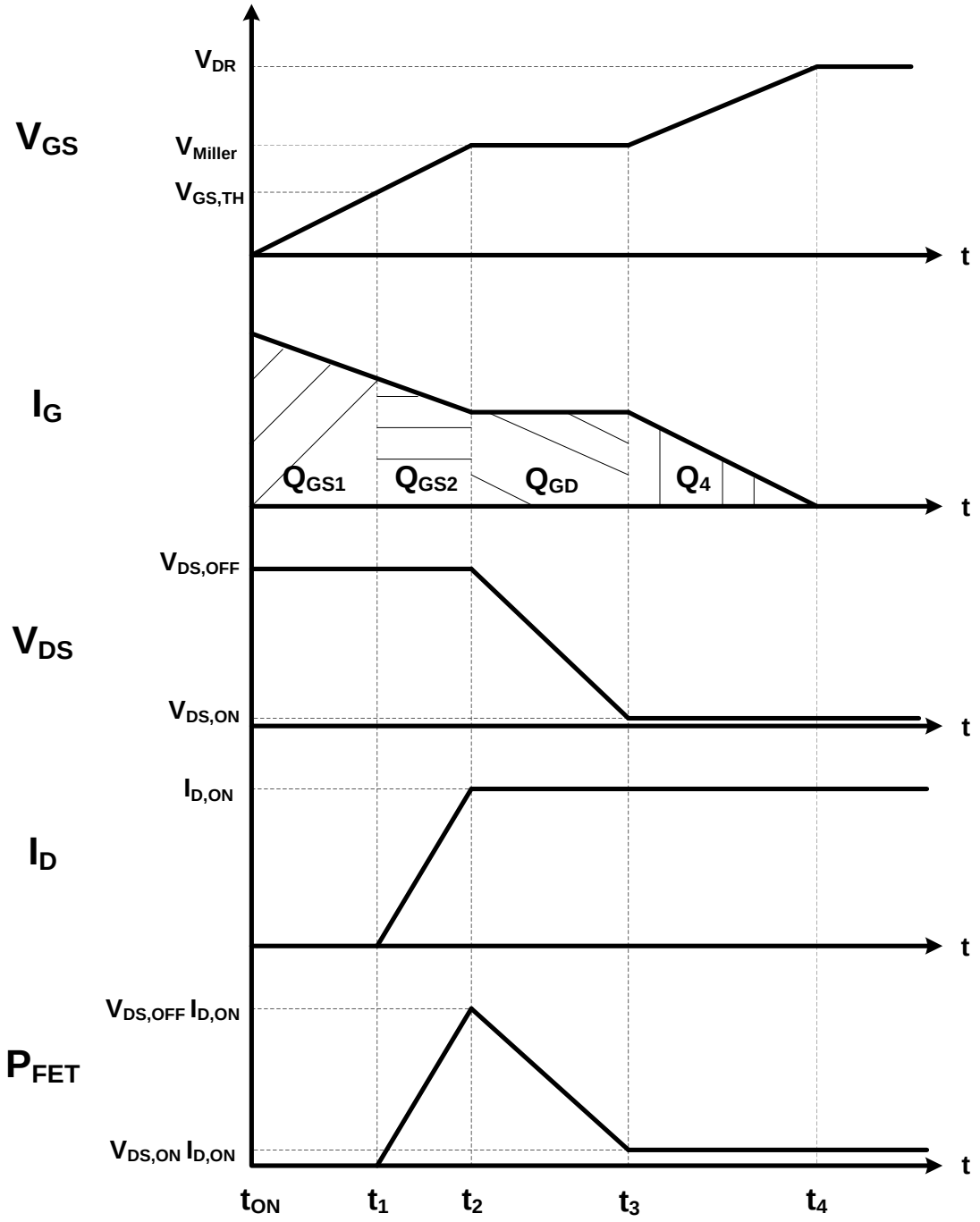



Figure 4.6: FET Idealized Turn-On Transient

The turn-on event starts with $V_{GS} = 0$, $I_D = 0$, $V_{DS} = V_{DS,OFF}$, and at $t = t_{ON}$ the drive voltage goes from zero to $V_{DR}$. With $C_{GS}$ uncharged, the gate current immediately jumps up (practically this will be limited by the stray inductance connected to the gate) and initiates charging both $C_{GS}$ and $C_{GD}$. At $t = t_1$, the gate voltage has built to the threshold voltage $V_{GS,TH}$ and the device can start conducting current. The interval from $t = t_{ON}$ to $t = t_1$ is termed the delay time and since no current is flowing through the FET, no power is being dissipated. The area underneath the gate current waveform, $Q_{GS1}$, represents the required gate charge. Once $V_{GS} = V_{GS,TH}$, current is diverted from the ideal diode to the drain of the FET (here we assume in a linear manner). The drain current builds to the "clamped inductor" value of $I_{D,ON}$ while $V_{GS}$ continues to build to the "Miller plateau voltage" denoted here as $V_{Miller}$. During $t_1$ to $t_2$, there is both a non-zero voltage across the FET drain-source and a non-zero drain current, so the device experiences power loss. The required gate charge to transition through this interval is designated $Q_{GS2}$.

Once $V_{GS} = V_{Miller}$, the gate voltage stays relatively constant so $C_{GS}$ is not being charged and the parasitic capacitor $C_{GD}$ is principally charged. The gate current becomes constant and as the voltage across $C_{GD}$ builds, the voltage across $C_{DS}$ falls (since KVL requires $-V_{GS} + V_{GD} + V_{DS} = 0$). "Miller time" concludes at $t = t_3$ when the drain-source voltage drops to near its final on-state value. The gate charge required during this interval is denoted as $Q_{GD}$ and since both $V_{DS}$ and $I_D$ are non-zero, there are device power losses.

From $t = t_3$ up to $t = t_4$, the capacitors $C_{GS}$ and $C_{GD}$ continue to get charged until $V_{GS}$ reaches its final steady-state value of $V_{DR}$ and the gate current drops to zero. During this interval the FET is ON and it is operating as a switch while the channel is being fully enhanced and $R_{DS,ON}$ is achieving its ON-state value. The required gate charge for this interval is $Q_4$. The aggregate charge $Q_{GS1} + Q_{GS2} + Q_{GD} + Q_4$ is what must be provided by the "gate driver" to turn the FET ON and clearly, the larger the gate current, the quicker we will be able to provide that charge.

We will denote the time required for the drain current to rise as $t_{IR} = t_2 - t_1$ while the time it takes for the drain-source voltage to fall is $t_{VF} = t_3 - t_2$. The combination of the two times will represent the amount of time associated with switching losses or when the drain current and drain-source voltage are transitioning states. Thus,

$$T_{SW,ON} = t_{IR} + t_{VF} \tag{4.1}$$

The process for turning the FET OFF is shown in Figure 4.7.

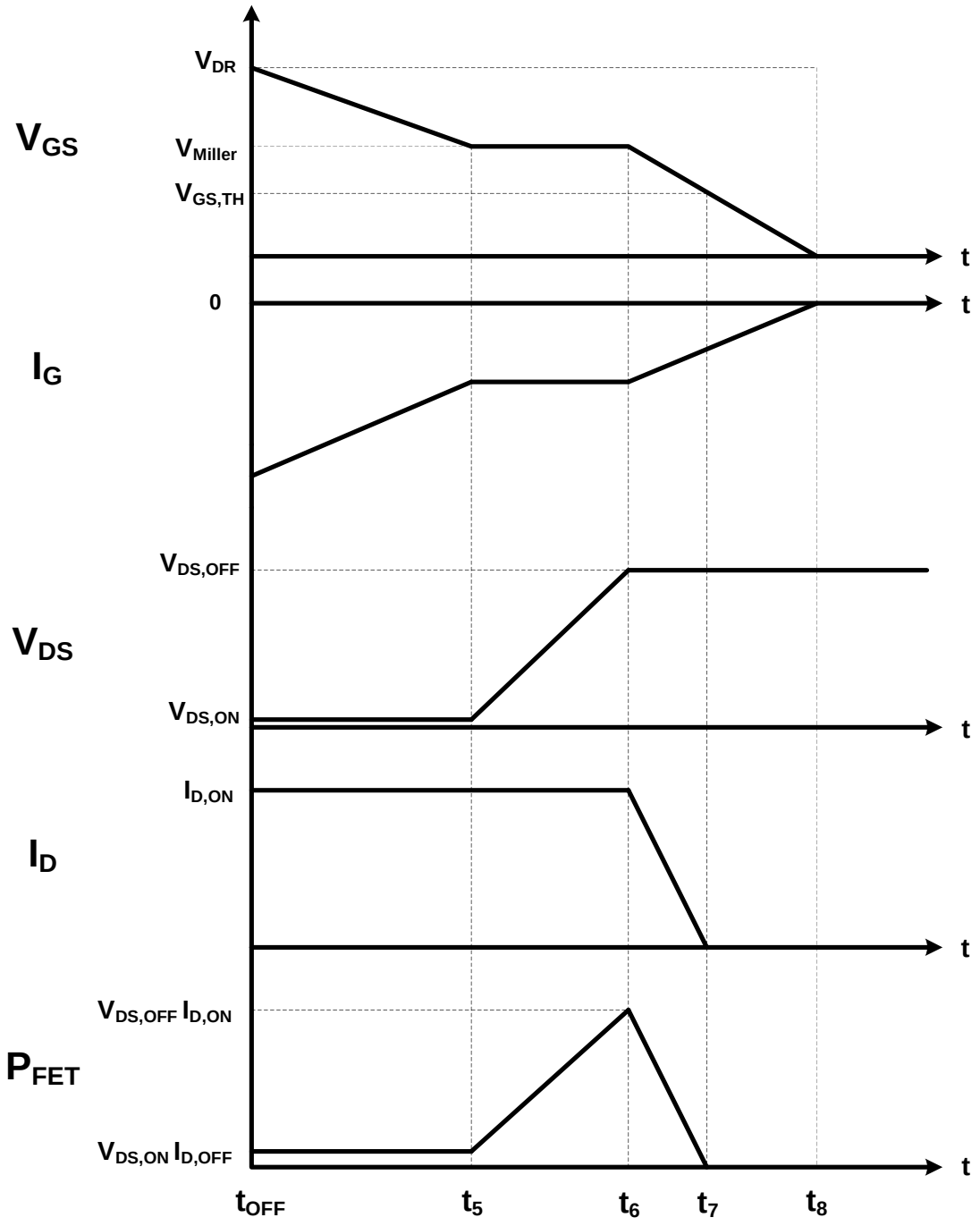



Figure 4.7: FET Idealized Turn-Off Transient

Here we start with $I_D = I_{D,ON}$, $V_{DS} = V_{DS,ON}$, $V_{GS} = V_{DR}$ and the drive voltage is set to zero at $t = t_{OFF}$. This initiates a large negative gate current which starts the process of discharging the FET parasitic capacitors $C_{GS}$ and $C_{GD}$. From $t = t_{OFF}$ until $t = t_5$, the voltage $V_{GS}$ falls from $V_{DR}$ to $V_{Miller}$. This represents turn-off delay time as the drain current or drain-source voltages have not yet started to change.

Once $V_{GS}$ is clamped at $V_{Miller}$, the capacitor $C_{GD}$ is discharging and thus $V_{DS}$ builds to its blocking voltage $V_{DS,OFF}$. The FET experiences power loss depending on this transient. Once $V_{DS} = V_{DS,OFF}$, the capacitor $C_{GS}$ continues to discharge and the gate-source voltage falls to the threshold voltage. This change in $V_{GS}$ causes an increase in the channel resistance and the drain current decreases, causing a shift of current from the FET to the ideal diode. This interval also represents a power loss transient. From $t = t_7$ until $t = t_8$, the device is OFF, but the final amount of charge must be pulled from $C_{GS}$ and $C_{GD}$ to pull the gate-source voltage down to zero to achieve steady state.

We will denote the time required for the drain-source voltage to rise as $t_{VR} = t_6 - t_5$ while the time it takes for the drain current to fall is $t_{IF} = t_7 - t_6$. The combination of the two times will represent the amount of time associated with turn-off switching losses or when the drain current and drain-source voltage are transitioning states. Thus,

$$T_{SW,OFF} = t_{VR} + t_{IF} \tag{4.2}$$

Therefore, the power dissipated in the FET appears as shown in Figure 4.8 where for illustration purposes we have exaggerated the amount of time that the switch is turning ON and OFF ($T_{SW,ON}$ and $T_{SW,OFF}$) relative to the switching period $T_{SW}$. The area under the curve is the amount of energy lost per cycle by the FET.

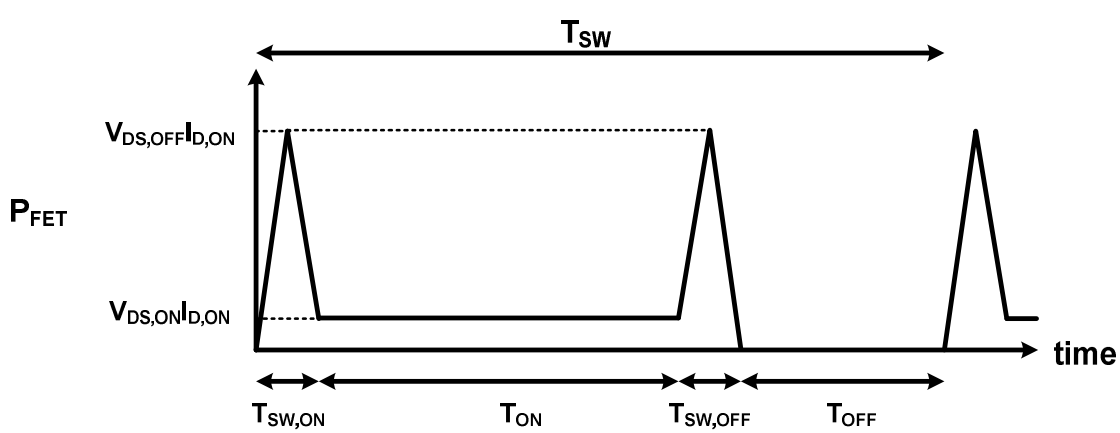



Figure 4.8: Approximate Power Lost by the FET during a Switching Cycle

To find the average power, we can find the area under the curve (the energy) and then divide by the switching period so that

$$P_{FET,ave} = \frac{E_{SW,ON} + E_{ON} + E_{SW,OFF}}{T_{SW}} \tag{4.3}$$

If we group the turn-on and turn-off energy losses, we can define the FET switching ($P_{FET,SW}$) and conduction ($P_{FET,Cond}$) losses

$$P_{FET,ave} = \frac{E_{SW,ON} + E_{SW,OFF}}{T_{SW}} + \frac{E_{ON}}{T_{SW}} = P_{FET,SW} + P_{FET,Cond} \tag{4.4}$$

Using the nearly triangular power characteristics during turn-on and turn off, we can get the average switching losses by

$$P_{FET,SW} = \frac{\frac{1}{2}V_{DS,OFF}I_{D,ON}T_{SW,ON} + \frac{1}{2}V_{DS,OFF}I_{D,ON}T_{SW,OFF}}{T_{SW}} = \frac{1}{2}V_{DS,OFF} \times f_{SW} \times I_{D,ON} \times \left(T_{SW,ON} + T_{SW,OFF}\right) \tag{4.5}$$

The conduction losses are determined by

$$P_{FET,Cond} = I_{D,rms}^2 \times R_{DS,ON} \tag{4.6}$$

which if we consider $D = T_{ON} / T_{SW}$ for Figure 4.8, this becomes

$$P_{FET,Cond} = DI_{D,ON}^2 \times R_{DS,ON} \tag{4.7}$$

So what we see is that the switching losses are directly dependent on how quickly we can turn ON/OFF the FET and the switching frequency. In contrast, the conduction losses are dependent on the current, channel resistance, and the duty cycle of the converter.

How do we have to modify equations (4.5) and (4.7) to represent buck chopper operation? First, consider the waveforms in Figure 4.9 where it is assumed that the switch turn-on and turn-off times are much smaller than the ON time. Note that the switch current $I_D$ will be larger at turn-off when the inductor current is maximum. Furthermore we see that the blocking voltage of the switch is $V_{in}$ so (4.5) becomes

$$P_{FET,SW} = \frac{1}{2}V_{in} \times f_{SW}\left(I_{L,\min} \times T_{SW,ON} + I_{L,\max} \times T_{SW,OFF}\right) \tag{4.8}$$

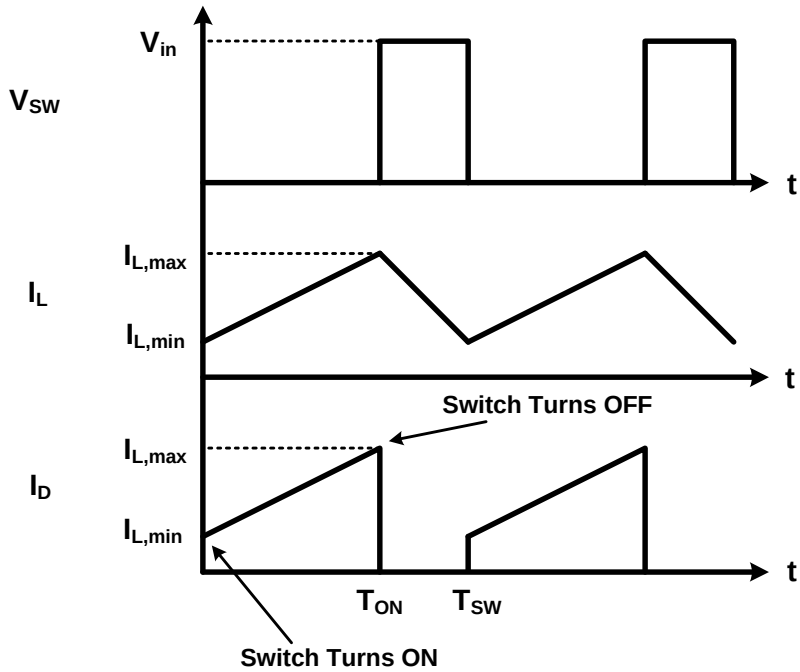



Figure 4.9: Buck Chopper Waveforms

For the conduction losses, we need to modify the expression for the rms value of the drain current. Since we are essentially weighting the rms value of the inductor current by the duty cycle, we are not surprised to find that

$$I_{D,rms} = \sqrt{D} I_{L,rms} \tag{4.9}$$

So that (4.6) becomes

$$P_{FET,Cond} = D \times I_{L,rms}^2 \times R_{DS,ON} \tag{4.10}$$

**<u>Example 4.1:</u>** Consider that we consider a buck chopper that steps 24V down to 12V. The rated output power is 100W and the critical power is selected to be 10W so that $I_{L,ave,\max} = 8.333A$ and $\Delta I_L = 1.667A$. The selected FET switch has $R_{DS,ON} = 50m\Omega$. Assume that the gate drive can achieve switch turn-on and turn-off times of 100ns. The resultant duty cycle is $D = 0.519$ and the switching frequency is 40kHz. Estimate the maximum average losses in the switch.

First, we need to calculate the maximum and minimum values of the inductor current and its rms value

$$I_{L,\max} = I_{L,ave} + \Delta I_L / 2 = 8.333A + (1.667A/2) = 9.17A$$

$$I_{L,\min} = I_{L,ave} - \Delta I_L / 2 = 8.333A - (1.667A/2) = 7.5A$$

$$I_{L,rms} = \sqrt{I_{L,ave}^2 + \left(\frac{\Delta I_L}{\sqrt{12}}\right)^2} = \sqrt{(8.333A)^2 + \left(1.667A/\sqrt{12}\right)^2} = 8.35A$$

We can then proceed to substitute into (4.10) to find the conduction losses

$$P_{FET,Cond} = D \times I_{L,rms}^2 \times R_{DS,ON} = 0.519 \times (8.35A)^2 \times 0.05\Omega = 1.809W$$

And the switching losses are found from (4.8) by

$$P_{FET,SW} = \frac{1}{2} V_{in} \times f_{SW} \left( I_{L,\min} \times T_{SW,ON} + I_{L,\max} \times T_{SW,OFF} \right) = \frac{1}{2} \times 24V \times 40kHz \times (7.5A + 9.17A) \times 100ns = 0.8W$$

The total average FET losses are the combination of the two results or

$$P_{FET,ave} = P_{FET,SW} + P_{FET,Cond} = 0.8W + 1.809W = 2.609W$$

We will find that this level of losses will most likely require a heat sink in order to avoid excessive heating of the device (and failure).

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Thus, (4.8) and (4.10) can be used to estimate the average losses in the buck chopper FET switch; however, to do so, we need to estimate the FET turn-on and turn-off times. Unfortunately, the data on rise and fall times for a FET given on the specification sheets are for a resistive load versus an inductive-clamped load and are for a specific operating point. Thus the trajectory change of $V_{DS}$ and $I_D$ can be significantly different then what occurs in a buck chopper. The way around this problem is to consider another data plot that the vendor provides: gate-source voltage versus gate charge as shown in Figure 4.10. The curve is generated by injecting a constant current into the gate so that one can integrate and find the accumulated charge while measuring the gate-source voltage.

This curve is sweet in that it contains all of the charge information that might be required without needing to know anything about time or how the parasitic capacitances are changing. That is, the same curve would apply whether the gate current is low and the switch times long or the gate current is high and the switch times are short. Now there typically is some operating point dependency involved with this curve which will be dependent on the off-state voltage that the FET must block (a family of curves are usually given with the variation occurring mainly in the $Q_4$ region. For the device shown the threshold voltage is 4V, the Miller plateau voltage is 6V, the drive voltage is 12V and we can deduce that $Q_{GS2} = 20nC - 16nC = 4nC$, $Q_{GD} = 100nC - 20nC = 80nC$, and the total charge required by the gate is $Q_G = 160nC$.

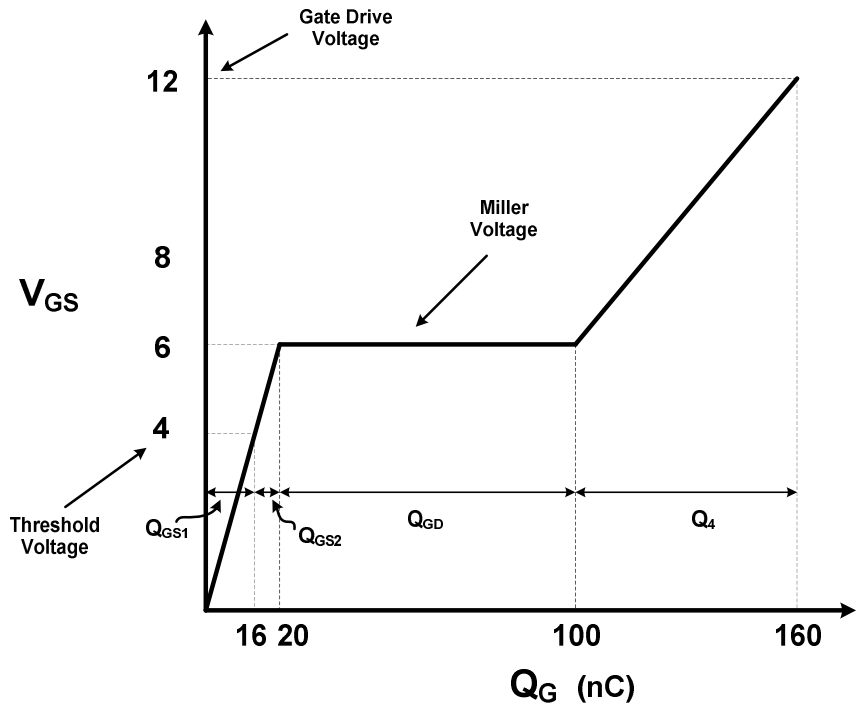



Figure 4.10: Representative Vendor-Provided $V_{GS}$ Versus Gate Charge Curve

OK, so how can we take that data and estimate the switch turn-on and turn-off times? First, we need to go back to Figures 4.6 and 4.7 and estimate values for $t_{IR}$, $t_{VF}$, $t_{IF}$, and $t_{VR}$. Well via Figure 4.6, we can estimate the gate-source voltage while the current is rising as $V_{GS} \approx \frac{V_{GS,TH} + V_{Miller}}{2}$, so the current will be on average $I_G \approx \frac{V_{DR} - V_{GS}}{R_{DR} + R_{Gext}}$. The charge is then estimated as being the average current multiplied by the time to give

$$I_{G,ave} \times \Delta t = \frac{V_{DR} - \left( \frac{V_{GS,TH} + V_{Miller}}{2} \right)}{R_{DR} + R_{Gext}} \times t_{IR} \approx Q_{GS2} \tag{4.11}$$

The voltage fall time is a bit easier as $V_{GS}$ is essentially constant at the Miller plateau and we get

$$\frac{V_{DR} - V_{Miller}}{R_{DR} + R_{Gext}} \times t_{VF} \approx Q_{GD} \tag{4.12}$$

Then the switch turn-on time is calculated from (4.1). To get the switch turn-off time, we first recognize that the drive voltage is set to zero and then observe the waveforms in Figure 4.7. The voltage rises while the gate-source voltage is at the Miller plateau so

$$\frac{V_{Miller}}{R_{DR}+R_{Gext}} \times t_{VR} \approx Q_{GD} \tag{4.13}$$

The current falls as the gate-source voltage transitions between the Miller plateau and the threshold voltage. We will once again use the average of these two points to find the average gate current, and then compute the charge transmitted

$$\frac{\left(\frac{V_{GS,TH}+V_{Miller}}{2}\right)}{R_{DR}+R_{Gext}} \times t_{IF} \approx Q_{GS2} \tag{4.14}$$

So we are arguing that given a FET, we can estimate $Q_{GS2}$, $Q_{GD}$, $V_{GS,TH}$, and $V_{Miller}$ from the data sheets. We will choose $V_{DR}$ and $R_{Gext}$, and $R_{DR}$ is a parameter of the driver circuit. The voltage $V_{DR}$ must be at least $2V_{GS,TH}$ but more probably no greater than 12V since $R_{DS,ON}$ will not get any smaller and you will only be increasing the total required charge of the driver (and you must also not exceed the gate breakdown voltage which is typically around 20V).

OK, so let's combine (4.11) and (4.12) together with (4.1) to derive an estimate for the switch turn-on time

$$T_{SW,ON} = t_{IR} + t_{VF} \approx \left(R_{DR}+R_{Gext}\right)\left[\frac{Q_{GS2}}{V_{DR}-\left(V_{GS,TH}+V_{Miller}\right)/2} + \frac{Q_{GD}}{V_{DR}-V_{Miller}}\right] \tag{4.15}$$

Similarly, we can combine (4.13) and (4.14) with (4.2) to derive an estimate for the switch turn-off time

$$T_{SW,OFF} = t_{IF} + t_{VR} \approx \left(R_{DR}+R_{Gext}\right)\left[\frac{Q_{GS2}}{\left(V_{GS,TH}+V_{Miller}\right)/2} + \frac{Q_{GD}}{V_{Miller}}\right] \tag{4.16}$$

We immediately notice that the switching times directly depend on the amount of charge $Q_{GS2}$ and $Q_{GD}$ required by the device. So if we wish to operate at high frequencies where we will need to switch very rapidly, these charge value must be small. We can further massage (4.15)-(4.16) by dividing through by the driver voltage to yield

$$T_{SW,ON} \approx \left(\frac{R_{DR}+R_{Gext}}{V_{DR}}\right)\left[\frac{Q_{GS2}}{1-\left(V_{GS,TH}+V_{Miller}\right)/2V_{DR}} + \frac{Q_{GD}}{1-(V_{Miller}/V_{DR})}\right] \tag{4.17}$$

$$T_{SW,OFF} \approx \left( \frac{R_{DR} + R_{Gext}}{V_{DR}} \right) \left[ \frac{Q_{GS2}}{\left(V_{GS,TH} + V_{Miller}\right)/2V_{DR}} + \frac{Q_{GD}}{(V_{Miller}/V_{DR})} \right] \tag{4.18}$$

What this reveals is that the term out front will be inversely related to the peak current going into the gate, which will be limited by what the driver circuit can provide. This makes sense: if we can supply more current, then the switching times should be shorter (since we can deposit or extract charge quicker).

So what about $R_{Gext}$? Well, we will find that it will get specified in part to limit the current supplied or sinked by the driver. The peak gate current will occur when the gate is uncharged when turning the FET ON and when the gate is fully charged when turning the FET off. In either case, the difference in the voltage across $R_{DR}$ and $R_{Gext}$ is $V_{DR}$ and so

$$\left| I_{G,\max} \right| = \frac{V_{DR}}{R_{DR} + R_{Gext}} \tag{4.19}$$

If the driver current is limited, we need to ensure that it is less than this value or that

$$\left| I_{DR,\max} \right| < \frac{V_{DR}}{R_{DR} + R_{Gext}} \tag{4.20}$$

That will enable us to estimate a value of $R_{Gext}$ which obviously must be a standard resistor value.

What about the power rating of this gate resistor and of the gate driver? Well let's call $Q_G$ the total charge that the driver must provide to turn on the FET and have the gate-source voltage build to $V_{DR}$ (see Fig. 10). Thus

$$Q_G = Q_{GS1} + Q_{GS2} + Q_{GD} + Q_4 \tag{4.21}$$

While the drive voltage is at $V_{DR}$, the energy it provides is given by

$$E_{DR,ON} = \int_{t_{ON}}^{t_4} V_{DR} I_G dt = V_{DR} \int_{t_{ON}}^{t_4} I_G dt = V_{DR} Q_G \tag{4.22}$$

Therefore the average power is found by dividing this energy by the switching period (which is equivalent to multiplying it by the switching frequency)

$$P_{DR,ON} = \frac{E_{DR,ON}}{T_{SW}} = V_{DR} Q_G f_{SW} \tag{4.23}$$

Since the driver output resistance and the external gate resistance are in series (see Fig. 4.4), this average power will be distributed between them based on the relative sizes of those resistances or

$$P_{RGext} = \frac{R_{Gext}}{R_{DR} + R_{Gext}} P_{DR,ON} \tag{4.24}$$

If the driver output resistance is unknown, then the value found in (4.23) can be used to estimate the power dissipated in both the driver and the external gate resistance.

**<u>Example 4.2:</u>** Let's suppose we consider implementing our FET switch from example 4.1 with the International Rectifier IRF530NPbF device. This is a 100V device with a room-temperature value of $R_{DS,ON} = 90m\Omega$, a minimum gate threshold voltage of $V_{GS,TH,\min} = 2V$, and a gate charge characteristic given by the following

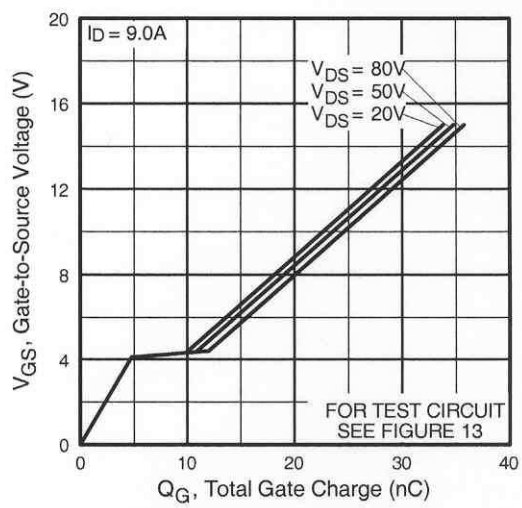
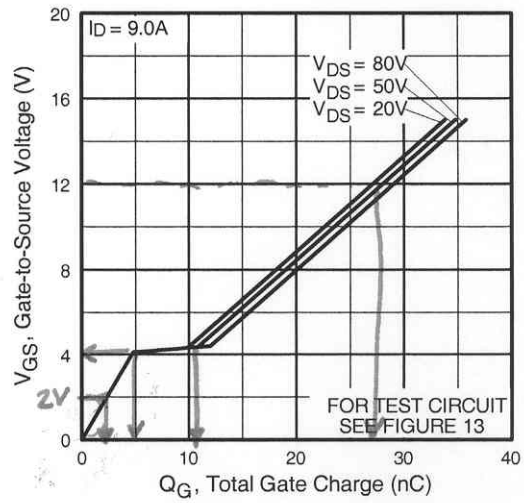



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

We will further assume that the drive voltage is set to 12V and that $R_{DR} + R_{Gext} = 12\Omega$. Determine estimates for the switch turn-on and turn-off times, the device losses, and the losses in the gate resistor.

First, we can identify from the gate charge characteristic the following quantities: $V_{Miller} = 4V$, $Q_{GS2} \approx 5nC - 2nC = 3nC$, $Q_{GD} = 11nC - 5nC = 6nC$, and $Q_G = 28nC$ based on the intersection of the 12V line with the characteristic between 20V and 50V since our input voltage from the example was 24V.




Next we can plug into (4.17) and (4.18) to estimate the switching times

$$T_{SW,ON} \approx \frac{12\Omega}{12V}\left[\frac{3nC}{1-\left(2V+4V\right)/(2\times 12V)}+\frac{6nC}{1-(4V/12V)}\right]\approx 13ns$$

$$T_{SW,OFF} \approx \frac{12\Omega}{12V}\left[\frac{3nC}{\left(2V+4V\right)/(2\times 12V)}+\frac{6nC}{(4V/12V)}\right]\approx 30ns$$

These are fairly aggressive switch times which could result in undesired $L\frac{\Delta I}{\Delta t}$ effects due to parasitic inductances. If we find that we would like to slow our FET down, we can be increasing $R_{Gext}$. For now we will leave it alone. As we did in Example 4.1, we can estimate the switching losses

$$P_{FET,SW} = \frac{1}{2}V_{in}\times f_{SW}\left(I_{L,\min}\times T_{SW,ON}+I_{L,\max}\times T_{SW,OFF}\right)=\frac{1}{2}\times 24V\times 40kHz\times\left(7.5A\times 13ns+9.17A\times 30ns\right)=0.18W$$

The conduction losses are now given by

$$P_{FET,Cond} = D\times I_{L,rms}^{2}\times R_{DS,ON} = 0.519\times\left(8.35A\right)^{2}\times 0.09\Omega\approx 3.26W$$

This is approximate because the on-state resistance was given to us at room temperature. The switching and conduction losses will tend to heat the device and cause the on-state resistance to increase. We will leave this dependency for a chapter down the road. Suffice it to say that this device appears to be able to switch at very high frequencies due to the low value of required gate charge.

Finally, a worst case estimate for the power consumed by the gate resistor is given by (4.23)

$$P_{DR,ON} \approx P_{Gext} = V_{DR} \times Q_G \times f_{SW} = 12V \times 28nC \times 40kHz = 0.013W$$

So a 1/8W resistor would be adequate.

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OK, so now that we have somewhat of an appreciation for characteristics of a “real” MOSFET switch, we next need to delve into the requirements and characteristics of a MOSFET gate driver!