5.0 MOSFET Gate Drivers

The location of the N-channel MOSFET in the buck chopper topology introduces a particular challenge to the power electronics engineer. As shown in Figure 5.1, the FET source terminal is not common with the gate voltage source V_G. The issue is exposed further by performing the KVL indicated in Figure 5.1.

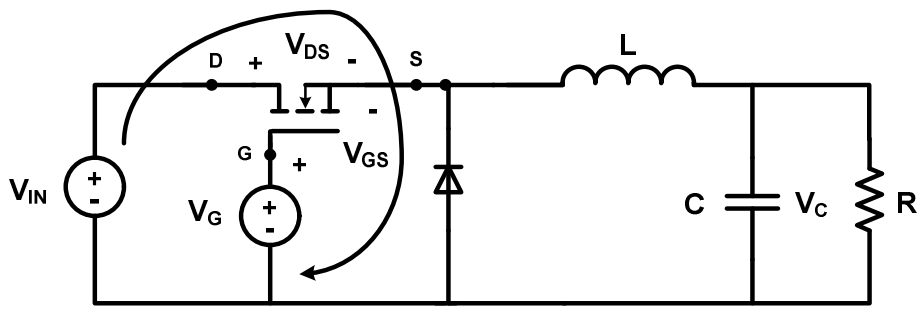

Figure 5.1: Illustration of Buck Chopper High-Side Switch

$$-V_{IN} + V_{DS} - V_{GS} + V_G = 0 \tag{5.1}$$

We can rearrange this expression to solve for the required gate voltage as

$$V_G = V_{IN} - V_{DS} + V_{GS} \tag{5.2}$$

If we desire that the FET be ON and behaving like a switch, then we require that the gate-source voltage be on the order of 10 to 12V. Further, by design we want the on-resistance of the FET to be small enough so that V_{DS} will be much smaller than either V_{IN} or V_{GS} so that (5.2) can be approximated by

$$V_G \approx V_{IN} + V_{GS} \tag{5.3}$$

This implies that the gate voltage must be 10 to 12V higher than the input voltage we are trying to "buck" down to a lower level. Thus if we had a 12V battery as an input, we would need to produce $V_G \approx +22V$ to turn the N-channel FET ON. Since we will typically derive many of our required auxiliary voltages from our input voltage, this poses a bit of a problem!

The first solution that we may consider is to replace the N-channel FET by a P-channel FET as shown in Figure 5.2. Here the source of the FET is connected to V_{IN} and the drain is connected to the buck inductor and diode. KVL about this circuit yields

$$V_G = V_{IN} + V_{GS} \tag{5.4}$$

To turn a P-channel FET ON, the gate-source voltage must go to -10V. Thus the gate voltage must vary between V_{IN} (FET OFF) and $V_{IN} - 10V$ (FET ON). As long as $V_{IN} > +10V$, we do not need a negative source and we can conceive of ways of doing this. Unfortunately though, the P-channel FET has characteristics that make this implementation less attractive.

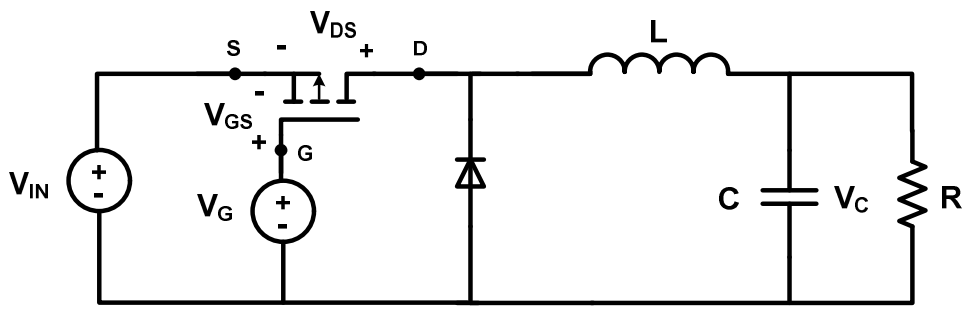

Figure 5.2: Buck Chopper Implemented with a P-Channel FET

P-channel MOSFETS are built on P-type epitaxial material where the majority carriers are *holes*. Since holes have lower mobility than electrons, the P-channel FET $R_{DS,ON}$ is two to three times larger than that of an N-channel FET of similar size. Thus a P-channel switch will have greater conduction losses and the buck converter will operate at a lower efficiency. We will also find that the similar-sized P-channel FET will cost more than the N-channel FET. As a result, we will defer considering the P-channel gate drive and move to overcoming the challenge of the N-channel switch.

To review, the issue with turning the N-channel FET ON in a buck topology is one of referencing. The source terminal of the FET is not at the common rail: it will float depending on the status of the FET. If the FET is ON, the source will be up near V_{IN}; if the FET is OFF, the source will be near 0V (as the diode conducts). Thus to turn the FET ON, we need to create an effective gate voltage that is higher than the input voltage.

One approach that solves this challenge is the *Boot-Strap circuit* shown in Figure 5.3.

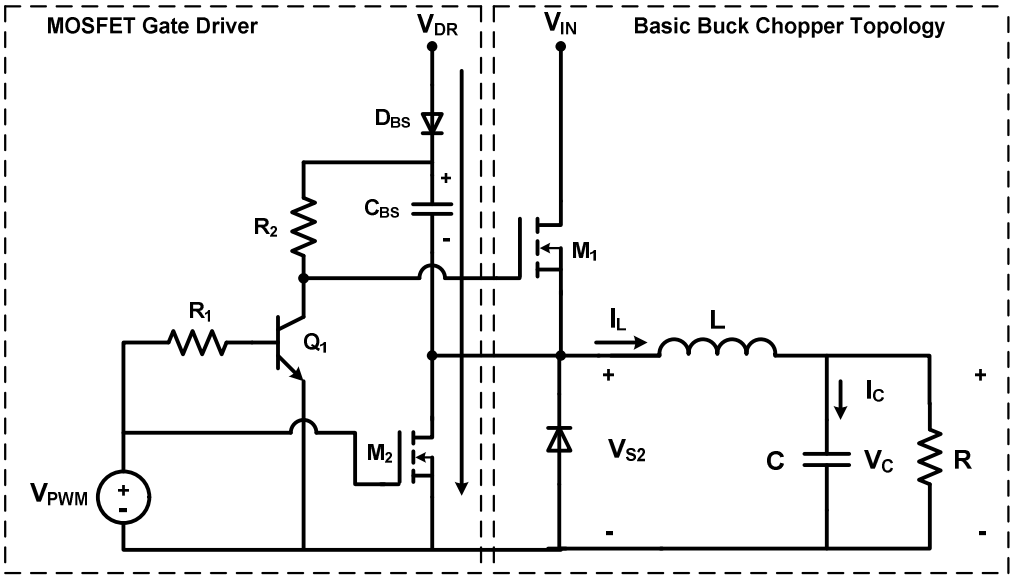

Figure 5.3: Buck Chopper with Boot-Strap High-Side Gate Driver

In this circuit, V_{PWM} is a duty cycle control voltage toggling between 0V and +5V. The voltage V_{DR} is the gate driver voltage that will typically be between +10V and +18V. The circuit operates as follows. When $V_{PWM} = +5V$, the driver transistors Q_1 and M_2 are ON. This connects the boot-strap capacitor C_{BS} and the gate of M_1 to the bottom rail (0V). Thus M_1 is OFF and C_{BS} charges up to V_{DR} via the boot-strap diode as shown in Figure 5.4.

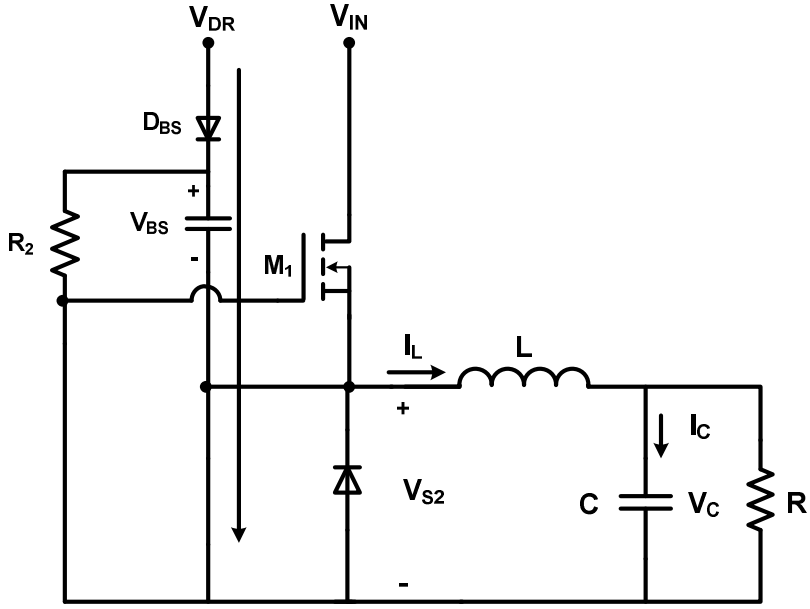

Figure 5.4: Main FET OFF and Boot-Strap Capacitor Recharges

When $V_{PWM} = 0V$, both Q_1 and M_2 turn OFF and the circuit becomes that shown in Figure 5.5.

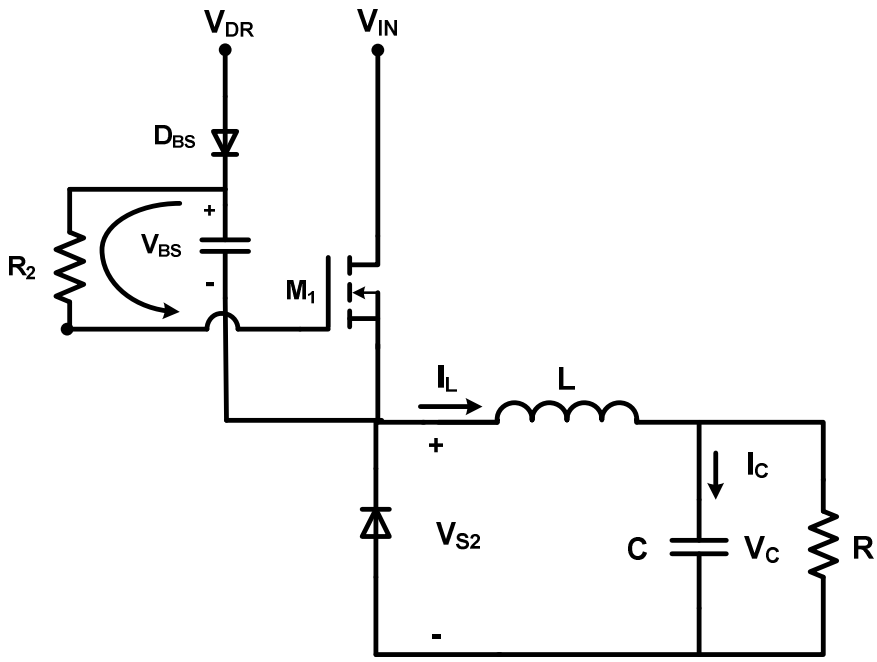

Figure 5.5: Boot-Strap Capacitor Discharges into Main FET Gate

The negative-side of the boot-strap capacitor is now connected to the source of M_1 while the positive-side is connected to the gate via R_2. C_{BS} begins to discharge, providing the gate current required to turn ON M_1. With M_1 ON, its source terminal voltage rises up to near V_{IN}. The diode D_{BS} then prevents the capacitor from discharging into V_{DR}. When we wish to turn M_1 OFF again, V_{PWM} goes to +5V, Q_1 and M_2 turn ON, the gate of M_1 is attached to ground, the M_1 gate capacitance discharges turning M_1 OFF, and C_{BS} recharges via V_{DR} and M_2. Thus the boot-strap capacitor requires the main switch to be OFF for some amount of time in order to replenish the charge lost while turning M_1 ON.

Many power electronic vendors provide Integrated Circuit (IC) chips that implement the boot-strap circuitry, though not necessarily using the exact circuit discussed above. International Rectifier (IR) provides several single high-side drivers as well as chips that implement both a high-side and a low-side driver as shown in Table 5.1. The example that we will consider here is the IR2117 driver and its recommended circuit layout is pictured in Figure 5.6.

Table 5.1 International Rectifier IC Gate Drivers

Device	I_{O+}	I_{O-}	V_{Power}	$V_{pwm,high}$	$V_{pwm,low}$	Q_{LS}	$I_{QBS,\max}$
IR2117	0.2A	0.42A	>9.6V	>9.5V	<6V	5nC	$240\mu A$
IR2125	1.0A	2.0A	>9.6V	>2.2V	<0.8V	5nC	1mA
IRS2110	2.0A	2.0A	>9.6V	>9.5V	<6V	5nC	$230\mu A$
IR2010	2.5A	2.5A	>9.7V	>2V	<1V	5nC	$210\mu A$
IRS2186	2.0A	2.0A	>9.8V	>2.5V	<0.8V	5nC	$150\mu A$

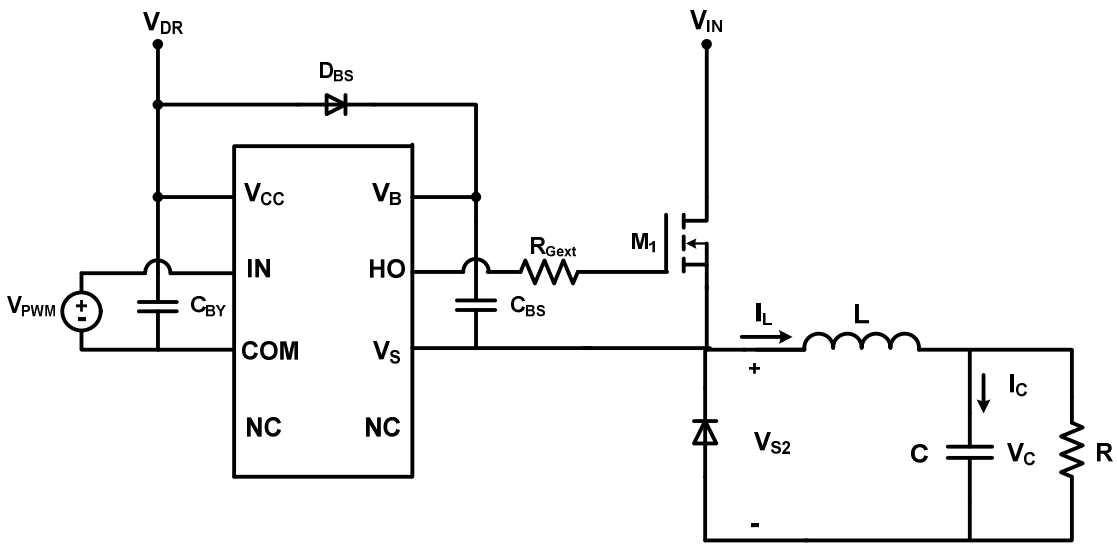

Figure 5.6: Buck Chopper with IR2117 High-Side Gate Driver

Here V_{DR} is the power supply voltage that we apply to the driver chip. The main FET M_1 is turned ON when V_{PWM} goes above 9.5V (not to exceed V_{DR}) and it is turned OFF when V_{PWM} goes below 6.0V (not to go below 0V). When we turn the main FET ON, the circuit that holds is shown in Figure 5.7. The boot-strap capacitor discharges into terminal V_B which then outputs through terminal HO to the gate of M_1. During this time, the capacitor current is governed by

$$I_{CBS} = C_{BS}\frac{dV_{BS}}{dt} \tag{5.5}$$

If we integrate this expression to find the change in charge over this time interval, we get

$$\Delta Q_{BS} = C_{BS}\Delta V_{BS} \tag{5.6}$$

We do not want the boot-strap capacitor voltage to dip too far while turning the FET ON, so we impose a requirement on the size of the capacitor

$$C_{BS,\min} = \frac{\Delta Q_{BS,\min}}{\Delta V_{BS,\max}} \tag{5.7}$$

where $\Delta Q_{BS,\min}$ is the minimum charge that the capacitor must supply to accomplish its task and $\Delta V_{BS,\max}$ is the maximum dip in the capacitor that is allowable. We determine the maximum allowable voltage dip by

$$\Delta V_{BS,\max} = \left(V_{DR} - V_{DBS} - V_{S2}\right) - V_{GS,\min} \tag{5.8}$$

where $V_{DR} - V_{DBS} - V_{S2}$ is the voltage that the boot-strap capacitor will charge up to (V_{DBS} is the voltage drop across the conducting boot-strap diode and V_{S2} is the voltage cathode-anode across the main buck chopper diode, thus it will be a negative value). For convenience, you can use V_{Miller} or $2V_{GS,TH}$ as the minimum gate-source voltage. For finding the change in charge, consider

$$\Delta Q_{BS,\min} = Q_G + Q_{LS} + \frac{I_{QBS\max}}{f_{SW}} + \frac{I_{CBSleak}}{f_{SW}} \tag{5.9}$$

Where Q_G is the total gate charge required for turn ON, Q_{LS} is the level-shift charge required by the driver (5nC for a 500/600V driver; 20nC for a 1200V driver), $I_{QBS\max}$ is the maximum current required by the floating section electronics of the driver (shown on the driver data sheet), $I_{CBSleak}$ is the boot-strap capacitor leakage current that decreases the voltage when the main FET is OFF (ceramic capacitors have extremely low leakage currents), and f_{SW} is the switching frequency. To ensure that we have much less than this worst-case voltage droop, we ensure some margin by providing a safety factor according to

$$C_{BS} = 15 C_{BS,\min} \tag{5.10}$$

We then choose the next highest standard-value capacitor.

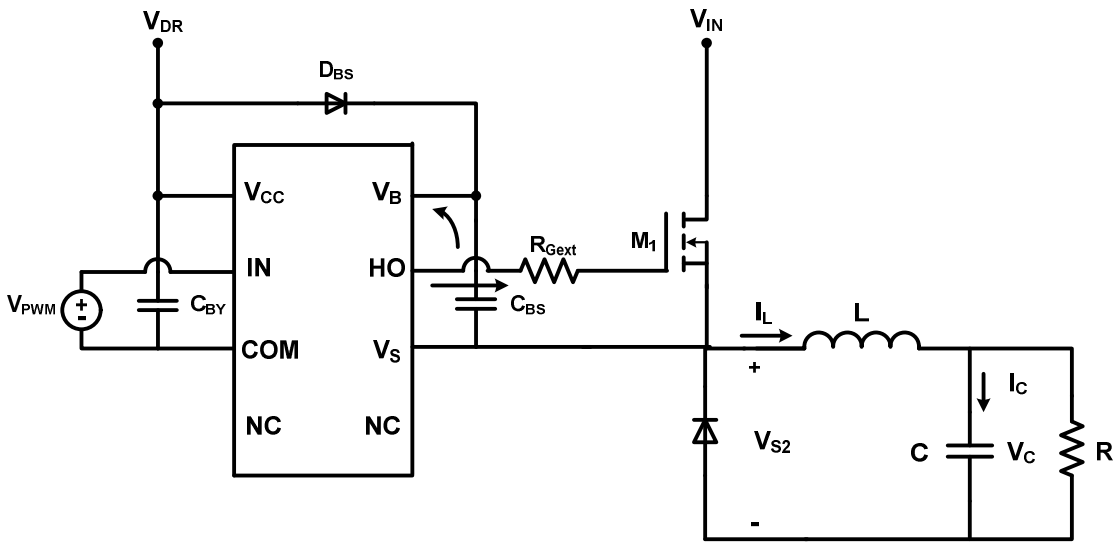

Figure 5.7: Discharge Path for Boot-Strap Capacitor

When V_{PWM} goes to its logical low state, the capacitor recharge path is shown in Figure 5.8. Note the path utilizes the main buck diode which exposes one issue with using this driver. Upon startup if only the diode is connected to M_1, there may not be a path available to supply the initial boot-strap capacitor charge to then turn on the main FET. We will also find that the boot-strap diode must be a *fast-recovery diode* so that its turn-off characteristics do not interfere with the charge provided to the main FET gate. It must be rated to handle at least an average current of

$$I_{DBS,ave} = \Delta Q_{BS,\min} f_{SW} \tag{5.11}$$

The capacitor C_{BY} which is connected between the driver supply voltage and ground should be sized to be at least one order of magnitude larger than the boot-strap capacitor. This capacitor will help to stiffen V_{DR} as the boot-strap capacitor gets recharged.

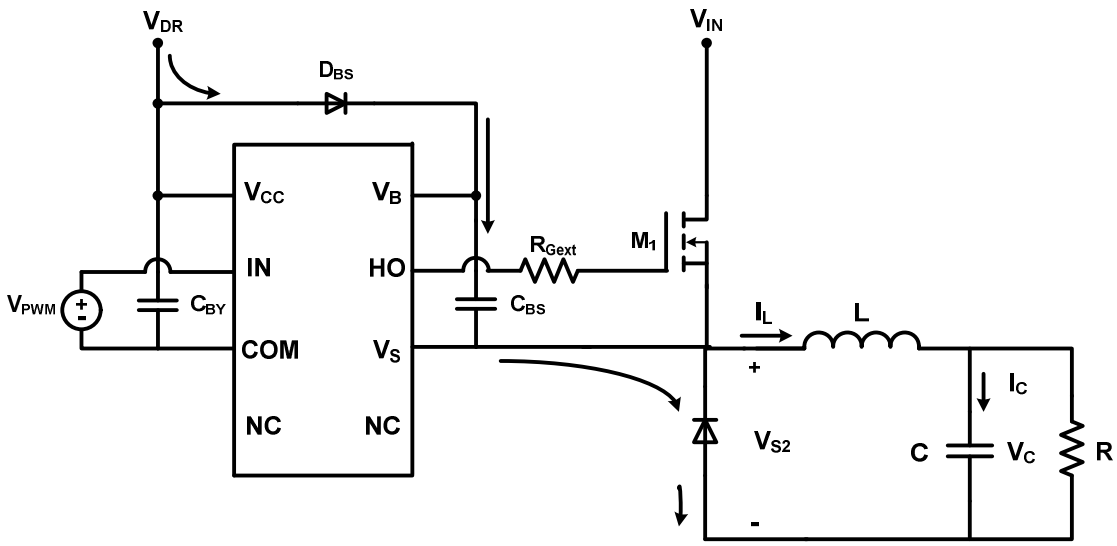

Figure 5.8: Boot-Strap Capacitor Recharge Path

Example 5.1: Let's suppose that we must design a high-side driver for some buck chopper application where the switching frequency has been selected to be 100kHz, the input voltage is 24V, and the gate drive voltage is 12V. Let's further assume that we have stipulated to using the IR2117 driver from International Rectifier and the FET has a threshold voltage of 4V, a Miller voltage of 6V, and requires a total of 40nC of gate charge at a gate drive voltage of 12V. The buck diode will have a drop of 1V. Find suitable values for the boot-strap circuit components.

Let's start with the external gate resistance. Since we have not been told anything about the internal gate resistance of the FET, we will assume it is zero for a worst-case estimate. The most current that the IR2117 driver can source is 0.2A, found in Table 5.1. Thus if we want to limit the current we need

$$R_{Gext} \geq \frac{V_{DR}}{I_{o+}} = \frac{12V}{0.2A} = 60\Omega$$

Recall, we would need to check that this level of current is adequate to achieve the switching times desired (using what we learned in Section 4). OK, on to the boot-strap circuit components. The maximum change in voltage across the boot-strap capacitor can be estimated as

$$\Delta V_{BS,\max} = \left(V_{DR} - V_{DBS} - V_{S2}\right) - V_{GS,\min} = 12V - 1V + 1V - 6V = 6V$$

Where we used the Miller voltage as being the minimum level we were allowing the voltage to drop to. The minimum charge that the boot-strap capacitor must provide is given by

$$\Delta Q_{BS,\min} = Q_G + Q_{LS} + \frac{I_{QBS\max}}{f_{SW}} + \frac{I_{CBSleak}}{f_{SW}} = 40nC + 5nC + \frac{240\mu A}{100kHz} + 0 = 47.4nC$$

if we assume that the capacitor leakage current is negligible. We can then use (5.7) and (5.10) to estimate the boot-strap capacitor as

$$C_{BS} = 15 \times \frac{\Delta Q_{BS,\min}}{\Delta V_{BS,\max}} = 15 \times \frac{47.4nC}{6V} = 0.12\mu F$$

Which we would scale to the next highest commercially-available value. The capacitance connected to the supply pin must be selected so that $C_{BY} > 10 \times C_{BS} = 1.1\mu F$. The boot strap diode must be able to safely conduct the following average current

$$I_{DBS,ave} = \Delta Q_{BS,\min} f_{SW} = 47.4nC \times 100kHz = 4.7mA$$

So this does not need to be a “big” device.

To this point, we have discussed the selection of the buck chopper inductor, capacitor, main switch, and gate driver. We still need to make some comments regarding the main diode.