7.0 Data Sheets and Device Selection

Data sheets for power transistors and diodes are packed with information, some of it is operating condition dependent and some of it is of dubious value. In order to reliably design a power electronic converter, you will need to understand the relative accuracy of your calculations and the appropriateness of your claims. In this section, we will perform an initial walk through of some data sheets and see what we find.

We will start with a typical N-channel power FET made by International Rectifier, part number IRF630NPBF. The top of the data sheet has the basic information shown in Figure 7.1. Note that in the circuit diagram, the FET is in parallel with the body diode that arises from the basic FET structure. The device is rated for 200V, 9.3A, and an on-resistance of 0.3Ω. This given voltage is the breakdown voltage and it should never be exceeded. A useful rule of thumb is to determine the maximum blocking voltage that the FET encounters in the power electronic application and then apply the following rule of thumb:

$$V_{rated} = 1.7V_{\max} \tag{7.1}$$

This ensures that a modest transient will not lead to device destruction. For a buck chopper topology, the maximum blocking voltage (when the device is OFF) is equal to the input voltage plus the main diode voltage drop.

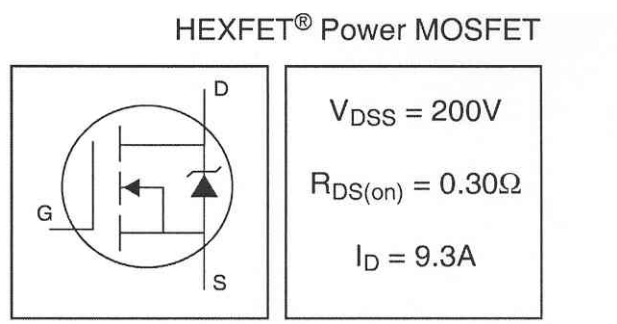

Figure 7.1: IRF630NPBF Device Rating

One must initially be cautious with the given value of on-resistance as this parameter will be temperature dependent as shown in Figure 7.2. What we notice is that if the device junction temperature increases to $160^{\circ}C$, the on-resistance will increase by a factor of about 2.75 (0.825Ω) and the conduction losses will increase similarly. We can keep track of this temperature dependency by fitting a line to the data and writing

$$R_{DS,ON}\left(T_J\right) = \frac{2.75-1}{160-25} \times R_{DS,ON}\left(25^{\circ}C\right) \times \left[T_J - 25^{\circ}C\right] + R_{DS,ON}\left(25^{\circ}C\right) \tag{7.2}$$

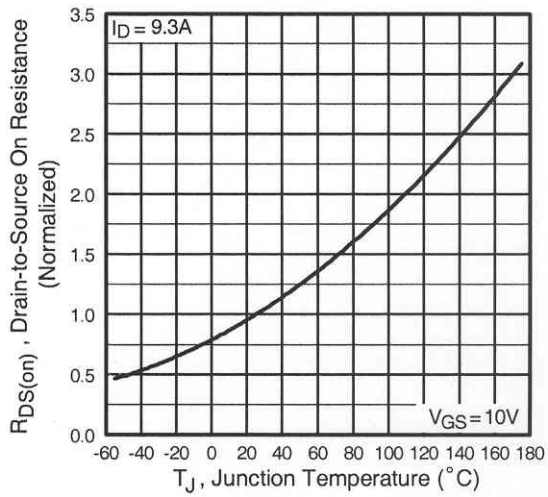

Figure 7.2: On-resistance versus Junction Temperature

Substituting that $R_{DS,ON}\left(25^{\circ}C\right) = 0.3\Omega$ leads to

$$R_{DS,ON}\left(T_J\right) = 0.00389\frac{\Omega}{^{\circ}C}\left[T_J - 25^{\circ}C\right] + 0.3\Omega \tag{7.3}$$

From a design perspective, you could simply choose a maximum junction temperature and use the corresponding on-resistance value as a worst case. If you actually operate at a lower temperature, then you will have fewer losses and your heat sink might be larger than required. Alternatively, you could iteratively use (7.3) within the design spread sheet.

We must next examine the FET current rating by digging into the chart shown in Figure 7.3.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.3	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	6.5	
I_{DM}	Pulsed Drain Current ①	37	
P_D @T_C = 25°C	Power Dissipation	82	W
	Linear Derating Factor	0.5	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy②	94	mJ
I_{AR}	Avalanche Current①	9.3	A
E_{AR}	Repetitive Avalanche Energy①	8.2	mJ
dv/dt	Peak Diode Recovery dv/dt ⑥	8.1	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew④	10 lbf•in (1.1N•m)	

Figure 7.3: FET Maximum Ratings

First, we note that the current rating of 9.3A is for *continuous current* at a case temperature of $25^{\circ}C$. The next value in the table shows that this current must be de-rated at higher temperatures. A buck chopper operates with a discontinuous current which on average can be estimated by

$$\eta_{buck} = \frac{P_{out}}{P_{in}} = \frac{V_{out,ave} I_{L,ave}}{V_{IN} I_{SW,ave}} \tag{7.4}$$

where η_{buck} is the efficiency of the converter expressed as a decimal. Using that $D \approx \frac{V_{out,ave}}{V_{in}}$ and solving for the average switch current, we get

$$I_{SW,ave} = \frac{D \times I_{L,ave}}{\eta_{buck}} \tag{7.5}$$

You can ballpark the efficiency to the 80-90% range and ensure that this value is less than the continuous rated value at the worst-case case temperature. Further as shown in Figure 7.3, the FET has $I_{DM} = 37A$. This is the maximum pulsed current. In a certain sense, both current values are a bit misleading in that ultimately power dissipation will determine whether a given drain current will be appropriate. Part of this is brought home by the safe operating area (SOA) data presented in Figure 7.4.

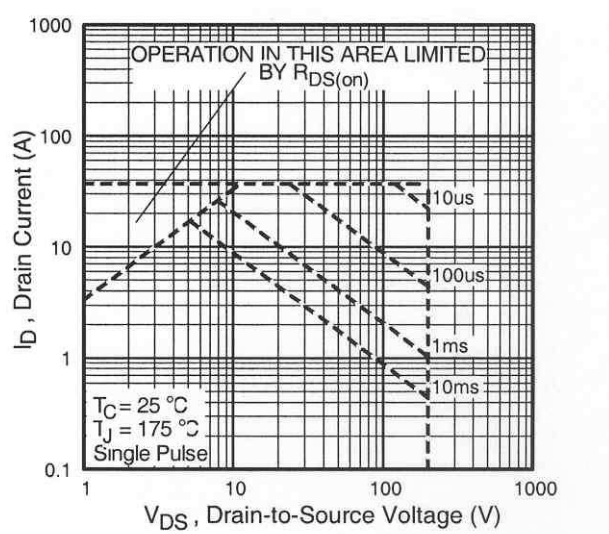

Figure 7.4: FET Safe Operating Area

Let's start with the outer rectangular. The horizontal boundary is at 37A, the peak pulsed current, while the vertical boundary is at 200V, the maximum blocking voltage. To consider what this curve is telling us, let's re-examine the "idealized" inductively-clamped switching transient introduced in Section 5 and presented here in Figure 7.5. Note during turn ON, the device starts with a high block voltage across it, the currents builds to its on-state value, and then the voltage falls to its on-state value (solid line of the trajectory). During turn OFF (dotted trajectory), the device voltage builds to its blocking value, and then the current falls to zero. Essentially this trajectory must fall within the device SOA while not exceeding its thermal capabilities (to be discussed in Section 8).

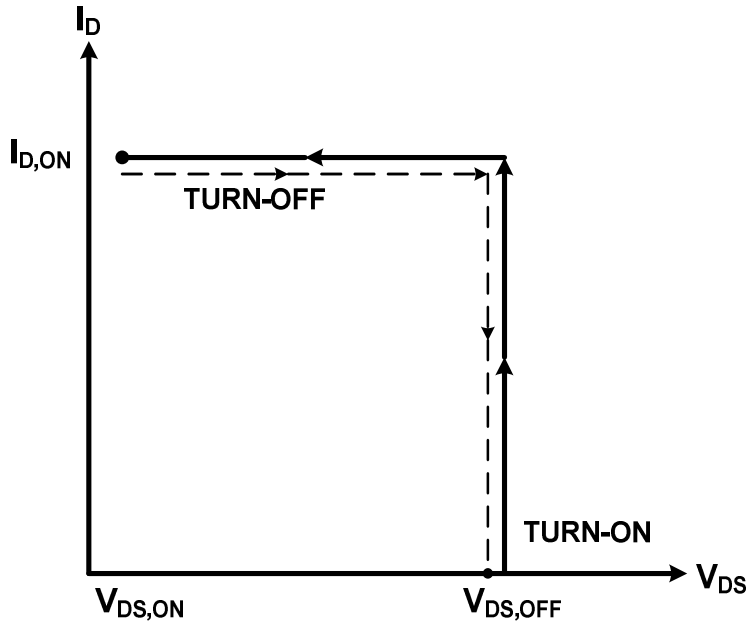

Figure 7.5: Idealized Turn-On and Turn-Off Buck Chopper Switch Trajectory

Now the trajectory in Figure 7.5 is at best idealized. A more realistic current-voltage trajectory is shown in Figure 7.6, where stray inductances and second-order effects can lead to overshoots and oscillations. The designer can build in margin in his/her design to accommodate these transients (as discussed with the voltage rating earlier) or may consider incorporating a snubber across the FET to reduce the overshoots. Snubber design is beyond the scope of this narrative. Suffice it to say that I_{DM} must not be exceeded and that the breakdown voltage must not be exceeded, all while the device thermal requirements are being obeyed. Before we leave the data shown in Figure 7.3, note that we also have listed the maximum gate-source voltage and the maximum allowable junction temperature: $V_{GS} < 20V$ and $T_J < 175^{\circ}C$. These are absolutes that must not be exceeded.

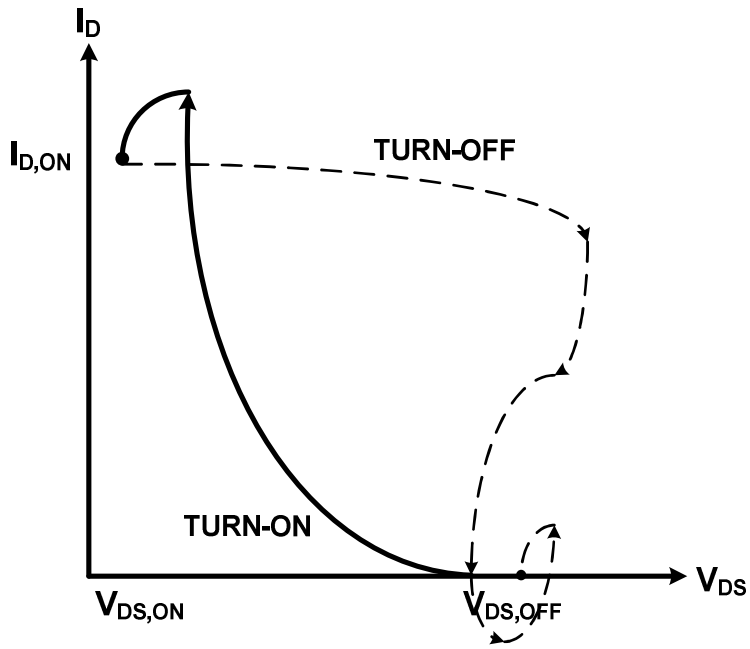

Figure 7.6: More Realistic Turn-On and Turn-Off Buck Chopper Switch Trajectory

Let's next consider the electrical characteristics of our FET as shown in Figure 7.7. Again we see the on-resistance value but now understand that this is at room temperature. Next the turn-on gate threshold voltage value is listed to be in the range of 2 to 4V. To ensure that we operate the FET as a switch, out of its linear mode where losses are high, we typically employ the following rule of thumb:

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

		Parameter	Min.	Typ.	Max.	Units	Conditions
	$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250μA
	$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I_D = 1mA
1	$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.30	Ω	V_{GS} = 10V, I_D = 5.4A ③
1	$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
	g_{fs}	Forward Transconductance	4.9	—	—	S	V_{DS} = 50V, I_D = 5.4A ③
	I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 200V, V_{GS} = 0V
			—	—	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
	I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
		Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
2	Q_g	Total Gate Charge	—	—	35	nC	I_D = 5.4A
2	Q_{gs}	Gate-to-Source Charge	—	—	6.5		V_{DS} = 160V
2	Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	17		V_{GS} = 10V ③
3	$t_{d(on)}$	Turn-On Delay Time	—	7.9	—	ns	V_{DD} = 100V
3	t_r	Rise Time	—	14	—		I_D = 5.4A
3	$t_{d(off)}$	Turn-Off Delay Time	—	27	—		R_G = 13Ω
3	t_f	Fall Time	—	15	—		R_D = 18Ω ③
	L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
	L_S	Internal Source Inductance	—	7.5	—		
	C_{iss}	Input Capacitance	—	575	—	pF	V_{GS} = 0V
	C_{oss}	Output Capacitance	—	89	—		V_{DS} = 25V
	C_{rss}	Reverse Transfer Capacitance	—	25	—		f = 1.0MHz

Figure 7.7: FET Electrical Characteristics

$$V_{GS} > 2V_{GS,TH,\max} \tag{7.6}$$

Thus for this device, a minimum value of 8V is advisable. Is more better? Let's consider the curves shown in Figure 7.8. The curves show drain current versus drain voltage and so the slope is related to the on-resistance. The curves are parameterized for different values of gate-source voltage, What we see is that for $V_{GS} > 8V$, the curves are nearly on top of each other and so there will be little difference in the final on-resistance values. Thus, more is NOT better as we will see that a higher gate-source voltage will necessitate more charge from the gate driver and more losses.

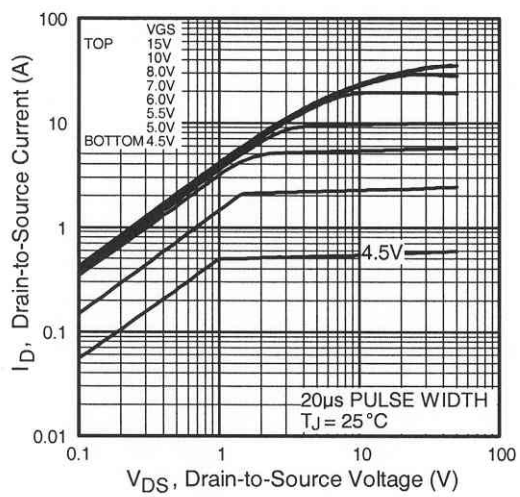

Figure 7.8: FET Drain Current versus Drain Voltage Characteristics

Also shown in Figure 7.7 is some maximum charge values: $Q_G = 35nC$, $Q_{GS} = 6.5nC$, and $Q_{GD} = 17nC$. This seems like "money" in that we can use them to find the switch-on and switch-off times as described previously. Hold it, these values are specific to $V_{GS} = 10V$ which we may or may not be using. Further, what are they (IR) considering Q_{GS} and Q_{GD}? Let's answer this question first as the data sheet defines this in Figure 7.9. So Q_{GS} is all of the gate charge up to the Miller plateau, Q_{GD} is the charge during "Miller time", and Q_G is the total charge up to when $V_{GS} = 10V$.

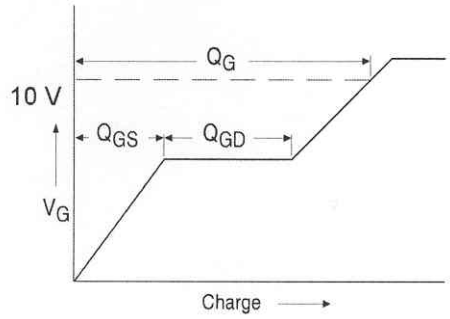

Figure 7.9: FET Charge Definitions

So why not directly use the charge curve provided in the data sheet and shown here as Figure 7.10? In this Figure we see that the curves are parameterized by blocking voltage which has an impact on when Miller time ends and the total charge required. This characteristic is for a continuous drain current of 5.4A and shows a Miller plateau voltage of roughly 5.5V. This curve predicts a gate charge of about 4.5nC to get to the Miller plateau, 8-11nC to get to the end of the Miller plateau (depending on the blocking voltage), and with 12V applied between 23-27nC of total charge (again depending on the blocking voltage of the application). These values are curiously lower than those from Figure 7.7 which appear to be worst case.

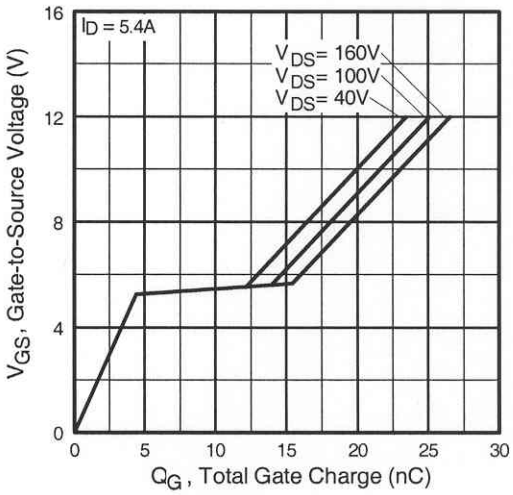

Figure 7.10: Gate-Source Voltage versus Gate Charge

One more item about Figure 7.11, the Miller plateau voltage can be estimated for different drain current using the following approximate relationship:

$$V_{Miller} \approx V_{GS,TH} + \frac{I_D}{g_{fs}} \tag{7.7}$$

where g_{fs} is the forward transconductance value that is found in Figure 7.7.

The last noteworthy items from Figure 7.7 are the switch times circled and identified as 3. Here we have turn-on and turn-off delay times, as well as rise and fall times. Unfortunately, the data corresponds to the test circuit shown in Figure 7.11. In this test circuit, the load is resistive and so the nature of the voltage-current trajectory can be significantly different than the inductive-clamped situation that is present in the buck chopper. Thus these values are of limited value and it is more prudent to live and die with the charge characteristic of Figure 7.10 to determine the switch times!

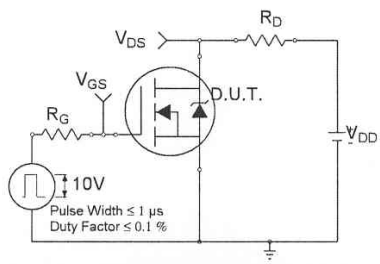

Fig 10a. Switching Time Test Circuit

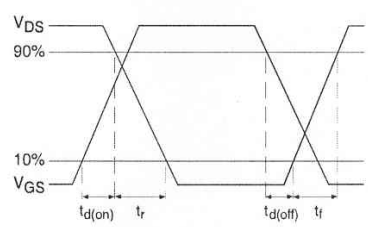

Fig 10b. Switching Time Waveforms

Figure 7.11: Resistive Load Circuit for Switch Times

The capacitance values in Figure 7.7 are also of limited use as the actual value is a function of voltage. Curves illustrating the change can be more useful but they do not facilitate initial design iterations.

There is other information provided on the FET data sheet, but this is a useful first pass through. Next, we will consider a fast-recovery diode data sheet for the International Rectifier part MUR820PBF shown in Figure 7.12.

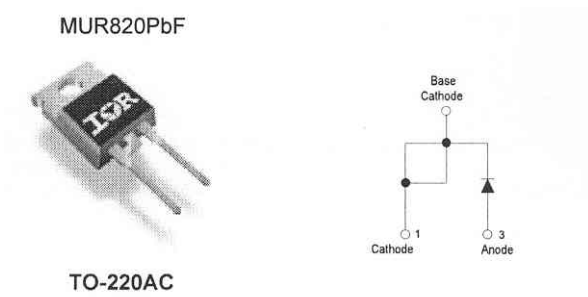

Figure 7.12: Fast-Recovery Diode

The absolute maximum device ratings are shown in Figure 7.13. Here $V_{RRM} = 200V$ is the maximum reverse-bias voltage that can be placed across the device. A similar de-rating as shown in Equation (7.1) may be applied to the blocking voltage. Three rated currents are given: the maximum average current ($I_{F(AV)} = 8A$), the peak repetitive forward current ($I_{FM} = 16A$), and the non-repetitive peak surge current ($I_{FSM} = 100A$). As the name implies, the non-repetitive surge current is a one-time event that must never be exceeded. During periodic transient conditions, I_{FM} must not be exceeded. For a buck converter, the diode carries the inductor current only when the switch is closed, so it is straightforward to show that the average diode current relates by

$$I_{dio,ave} = (1-D)I_{L,ave} \tag{7.8}$$

while the steady-state peak diode current would be

$$I_{dio,pk} = I_{L,\max} \tag{7.9}$$

The designer must further evaluate the diode power losses to ensure that the dissipation can be handled by appropriate thermal management techniques. Figure 7.13 also shows that the peak junction temperature must not exceed $175^{\circ}C$ (an important parameter in making those thermal management decisions).

Absolute Maximum Ratings

	Parameters	Max	Units
V_{RRM}	Peak Repetitive Peak Reverse Voltage	200	V
$I_{F(AV)}$	Average Rectified Forward Current Total Device, (Rated V_R), T_C = 150°C	8	A
I_{FSM}	Non Repetitive Peak Surge Current	100	
I_{FM}	Peak Repetitive Forward Current (Rated V_R, Square wave, 20 KHz), T_C = 150°C	16	
T_J, T_{STG}	Operating Junction and Storage Temperatures	-65 to 175	°C

Figure 7.13: Diode maximum Ratings

The maximum forward voltage drop is documented in Figure 7.14 for maximum average current at both room temperature and at $150^{\circ}C$. This could be the worst-case value that you might consider or you could go to the detailed IV-characteristic shown in Figure 7.15.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameters	Min	Typ	Max	Units	Test Conditions
V_{BR}, V_r	Breakdown Voltage, Blocking Voltage	200	-	-	V	I_R = 100μA
V_F	Forward Voltage	-	-	0.975	V	I_F = 8A
		-	-	0.895	V	I_F = 8A, T_J = 150°C
I_R	Reverse Leakage Current	-	-	5	μA	V_R = V_R Rated
		-	-	250	μA	T_J = 150°C, V_R = V_R Rated
C_T	Junction Capacitance	-	25	-	pF	V_R = 200V
L_S	Series Inductance	-	8.0	-	nH	Measured lead to lead 5mm from package body

Figure 7.14: Diode Electrical Characteristics

Here, you might either pick off the value corresponding to the expected maximum average current or you could fit the data to a straight line like

$$V_F = 0.0443 I_F + 0.35V = R_T I_F + V_T \tag{7.10}$$

where R_T and V_T would constitute a resistor/voltage source model of the conducting diode. Another important factor from Figure 7.14 is the reverse leakage current. Here it is in micro-amps so the resulting power loss will be small even if the diode was blocking rated voltage. This parameter is far more important when considering Schottky diodes which have significant leakage currents. For a buck, the reverse power loss would be evaluated as

$$P_{dio,rev} = V_R I_R D \tag{7.11}$$

The next pieces of data that are important for diodes are the reverse recovery characteristics shown in Figure 7.16. If nothing else this data shows that the three parameters associated with reverse recovery, the recovery time, charge and peak current, are all strongly dependent on the operating conditions. So let's look at the graphs provided in the data sheet, shown here as Figure 7.17. First we see that the data is temperature dependent: the recovery time and charge both increase with temperature (so probably use the $125^{\circ}C$ data as worst case). Next the curves are parameterized based on the rate of change of the forward current going through zero (dI_F / dt). This rate of change is set by the FET current rise time which is in turn influenced by the driver and external gate resistance. The faster we try to turn the FET ON, the shorter the recovery time and the greater the recovery charge.

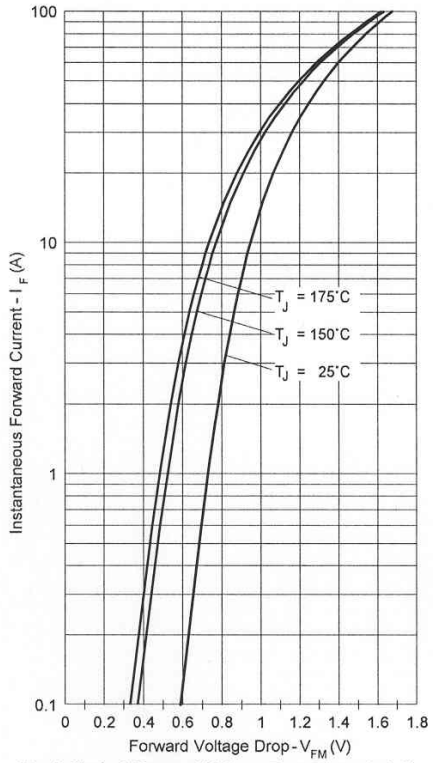

Fig. 1 - Typical Forward Voltage Drop Characteristics

Figure 7.15: Diode IV-Characteristics

Dynamic Recovery Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameters	Min	Typ	Max	Units	Test Conditions	
t_{rr}	Reverse Recovery Time	-	-	35	ns	I_F = 1.0A, di_F/dt = 50A/µs, V_R = 30V	
		-	-	25		I_F = 0.5A, I_R = 1.0A, I_{REC} = 0.25A	
		-	20	-		T_J = 25°C	I_F = 8A V_R = 160V di_F/dt = 200A/µs
			34			T_J = 125°C	
I_{RRM}	Peak Recovery Current	-	1.7	-	A	T_J = 25°C	
		-	4.2	-		T_J = 125°C	
Q_{rr}	Reverse Recovery Charge	-	23	-	nC	T_J = 25°C	
			-	75	-	T_J = 125°C	

Figure 7.16: Diode Reverse Recovery Tabulated Data

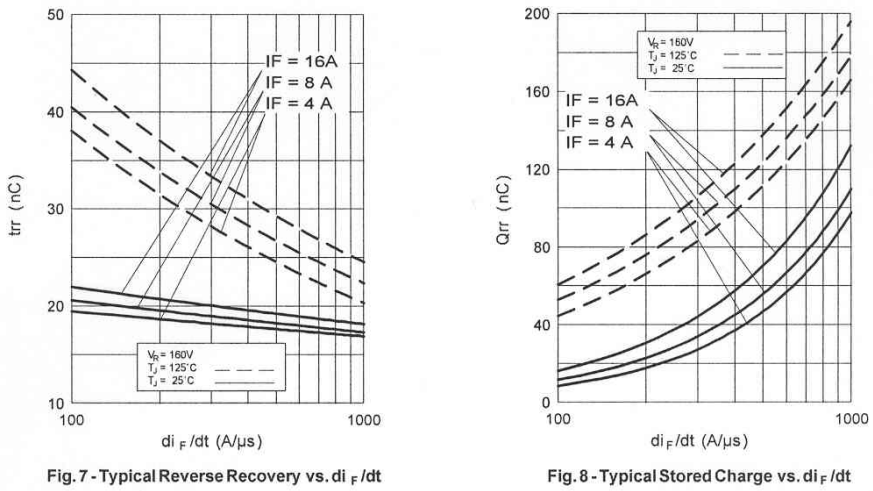

Fig. 7 - Typical Reverse Recovery vs. di F /dt

Fig. 8 - Typical Stored Charge vs. di F /dt

Figure 7.17: Diode Reverse Recovery Graphs

The peak recovery current is then related to the charge and time by

$$Q_{rr} \approx \frac{1}{2} t_{rr} I_{RRM} \tag{7.12}$$