8.0 Heat Management

What does it mean when we say that a FET or Schottky diode has power losses and how do we ensure that these losses do not lead to component failure? Switching and conduction losses within a semiconductor manifest as thermal energy injected into the part near the various PN-junctions. This thermal energy tends to raise the junction temperatures above that of the ambient (room) temperature. Above some critical junction temperature, $T_{j,\max}$, the semiconductor material begins to breakdown and the device fails. Thermal management refers to the strategies involved in removing the "waste heat" from the device and transferring it to the atmosphere. This subject is an entire course unto itself, so we will at best attempt to scratch the surface in this introduction!

Three modes are available to transfer heat between objects:

1. *Conduction*: transfer of heat energy between two solid objects in direct contact (an example is a heat sink)
2. *Convection*: transfer of heat energy from a hot surface to a moving fluid at a lower temperature (examples include forced-air cooling with a fan or closed-loop water cooling)
3. *Radiation*: transfer of heat energy in the form of electromagnetic waves between two surfaces of different temperature (for example, black objects maximize this form of heat transfer).

Conduction and convection are the dominant methods of removing heat from power converters, so we will focus mostly on these, but note that heat sinks and semiconductor parts are typically made black to maximize the smaller radiation effect. To analyze thermal systems, we need to introduce some basic concepts. Just as voltage is the force that pushes current through an electric circuit, temperature difference is the force that pushes heat from a warmer body to a cooler body. The flow of heat is measured in Watts. As the temperature difference increases, the amount of heat flow increases which leads us to the thermal analog to Ohm's Law

$$\Delta T = P_{diss} R_{\Theta} \tag{8.1}$$

In (8.1), ΔT is the temperature difference in units of $^{\circ}C$, P_{diss} is the heat flow in W, and R_{Θ} is the thermal resistance of the path in $^{\circ}C/W$. A small thermal resistance indicates that it is "easy" to pass heat through this path and it requires a small temperature difference. The thermal resistance depends on the physical properties of the objects and their geometry.

Consider the example of a semiconductor part mounted to a heat sink as shown in Figure 8.1. Heat is generated at the PN junctions of the part and then transmitted to the ambient environment through the device case, the mounting used to secure the case to the heat sink, and then finally the heat sink. "Temperature drops" occur from the junction to the case, from the case to the heat sink, and then from the heat sink to the ambient

environment. We can model the steady-state using the "electrical equivalent circuit" shown in Figure 8.2.

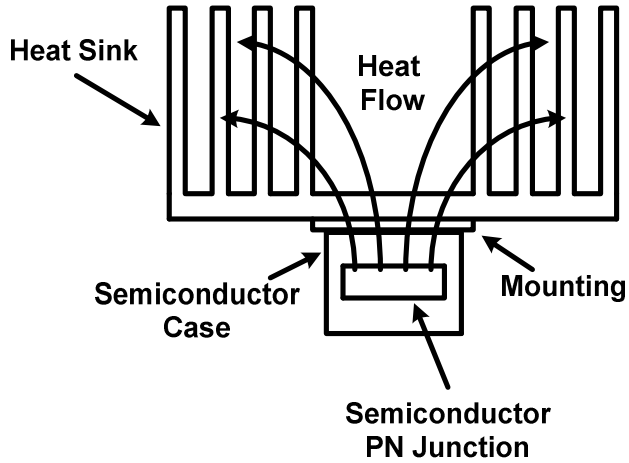


Figure 8.1: Semiconductor Part Mounted to a Heat Sink

The current source P_{diss} represents the power lost in the semiconductor part that shows up as heat that must flow to the ambient. The thermal resistances shown in Figure 8.2 represent the different material between the PN junction and the ambient.

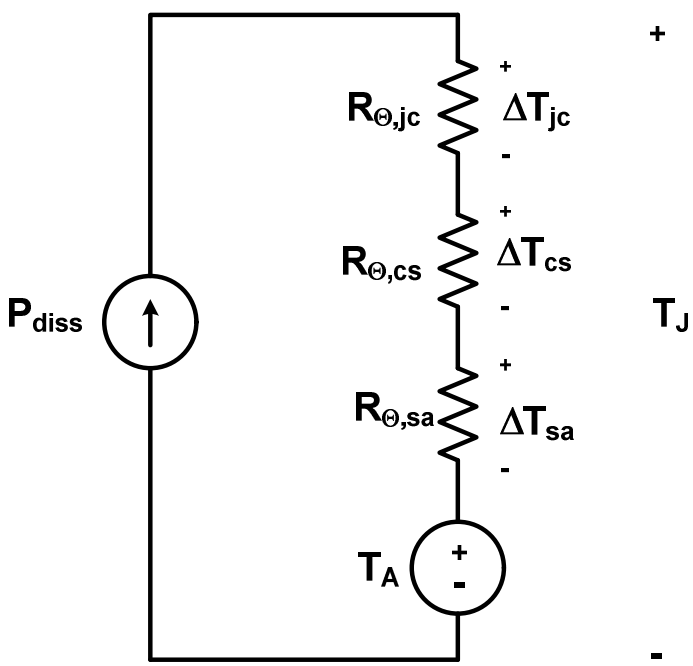


Figure 8.2: Electrical Equivalent Circuit of the Thermal System Shown in Figure 8.1

Specifically,

- $R_{\Theta,jc}$ is the thermal resistance from the silicon junction to the package case. This value is normally provided by the semiconductor device manufacturer on the data sheet
- $R_{\Theta,cs}$ is the thermal resistance of the interface material between the device package and the heat sink. This may include silicon grease or mounting pads (examples are sil pads or delta pads). Typical values can be found from heat sink manufacturers with some listed in Table 8.1.
- $R_{\Theta,sa}$ is the thermal resistance of the heat sink. Its value depends on the volume and geometry of the heat sink and is provided by the vendor.

Roughly speaking, the thermal resistance is estimated as follows

$$R_{\Theta} = \frac{t}{kA_C} \tag{8.2}$$

where 't' is the thickness of the resistance path in m, A_C is the contact area in m^2, and k is the thermal conductivity in $\frac{W}{m^{\circ}C}$. If we wish to create a small thermal resistance, then it requires a lot of contact area – this is why heat sinks typically utilize fins.

What is the circuit of Figure 8.2 saying? First, the ambient temperature is represented by the fixed DC voltage source. We are assuming that the power converter is not generating enough waste heat to change the temperature of the room. The flow of heat from the part then creates temperature drops across each thermal resistance, ΔT_{jc}, ΔT_{cs} and ΔT_{sa}. The temperature at the junction is then simply the sum of these temperature drops and the ambient temperature

$$T_J = \Delta T_{jc} + \Delta T_{cs} + \Delta T_{sa} + T_A \tag{8.3}$$

If we substitute the "Thermal Ohm's Law" of Equation (8.1), we get

$$T_J = \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}\right)P_{diss} + T_A \tag{8.4}$$

Since $R_{\Theta,jc}$ is determined once we have selected our semiconductor part and $R_{\Theta,cs}$ is known once we have decided on how we intend to mount the part to the heat sink, the only item not specified in (8.3) is the heat sink thermal resistance, so let's solve for it.

$$R_{\Theta,sa} = \frac{T_J - T_A}{P_{diss}} - R_{\Theta,jc} - R_{\Theta,cs} \tag{8.5}$$

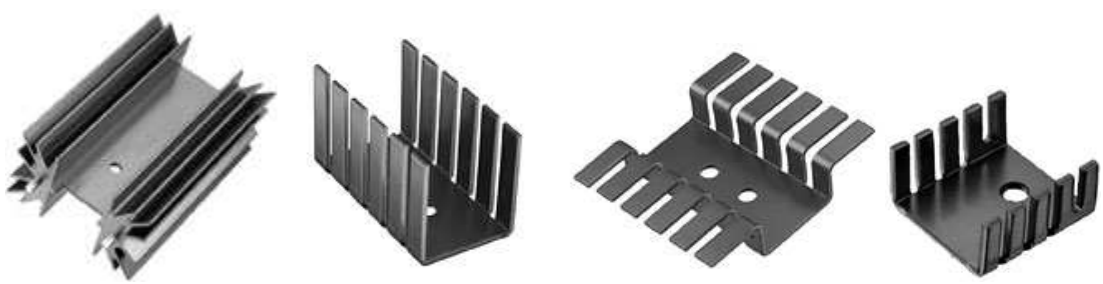
The most constraining situation is when the ambient temperature is the largest (we can afford the minimum temperature drops across the thermal resistances). Thus we can solve for the maximum allowable heat sink thermal resistance using

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss}} - R_{\Theta,jc} - R_{\Theta,cs} \tag{8.6}$$

Any heat sink thermal resistance smaller than this value will ensure a silicon junction temperature less than $T_{J,\max}$. Recall $T_{J,\max}$ is a well-defined value for any part. A collection of heat sinks are shown in Figure 8.3. Note to achieve a smaller value of $R_{\Theta,sa}$, greater surface area and heat sink volume is required.

Table 8.1: Thermal Resistance of Typical Semiconductor Mounting Material

Mounting Medium	**Typical $R_{\Theta,cs}$ ($^\circ C/W$)**
Wakefield thermal compound	0.1 - 0.2
Beryllia washer	0.2
Wakefield delta pads	0.25 – 0.5 in^2
Mica washer	0.5
Kapton	0.4
Sil pads	0.4 in^2



$R_{\Theta,sa} = 2.6^\circ C/W$ $R_{\Theta,sa} = 3.7^\circ C/W$ $R_{\Theta,sa} = 6.4^\circ C/W$ $R_{\Theta,sa} = 24^\circ C/W$

Figure 8.3: Typical Aluminum Heat Sinks and Thermal Resistance Values

What if no heat sink is used? The semiconductor part manufacturer also gives you a value indicating the effective thermal resistance between the junction and the ambient such as shown in Figure 8.4 for the IRF630 power MOSFET.

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.83	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient④	—	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)⑤	—	40	

Figure 8.4: Thermal Data for the IRF630 Power MOSFET

Here data is provided for the cases where the part is mounted to a PC board or not. Let's consider the situation where the part is <u>not</u> mounted to a board and that we wish to maintain $T_J < 150^\circ C$ while considering a maximum ambient temperature of $50^\circ C$ ($122^\circ F$), we can rewrite (8.4) as

$$T_{J,\max} = R_{\Theta,ja} P_{diss,\max} + T_{A,\max} \tag{8.7}$$

Then solve for the maximum power this part could safely dissipate without a heat sink

$$P_{diss,\max} = \frac{T_{J,\max} - T_{A,\max}}{R_{\Theta,ja}} = \frac{150^\circ C - 50^\circ C}{62^\circ C/W} = 1.61W \tag{8.8}$$

Let's next assume that we need to dissipate 10W in this part. This tells us that we require a heat sink and we can use Equation (8.6) and the data from Figure (8.4) to determine the maximum thermal resistance of the heat sink

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss}} - R_{\Theta,jc} - R_{\Theta,cs} = \frac{150^\circ C - 50^\circ C}{10W} - 1.83^\circ C/W - 0.5^\circ C/W = 7.67^\circ C/W \tag{8.9}$$

We could use any of the leftmost three heat sinks in Figure 8.3. If we allow a higher junction temperature or a lower maximum ambient temperature, then we could conceivably use a smaller (and less expensive) heat sink (though the rightmost heat sink in Figure 8.3 is not a possibility). Another way to view this is let's assume that we have an "ideal" heat sink with $R_{\Theta,sa} = 0^\circ C/W$ (like the outside hull of a submarine) and solve for the maximum power that we can dissipate

$$P_{diss,\max} = \frac{T_{J,\max} - T_{A,\max}}{R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}} = \frac{150^\circ C - 50^\circ C}{(1.83 + 0.5 + 0)^\circ C/W} = 42.9W \tag{8.10}$$

which starts to provide a handle as to what the maximum power capability is for a TO-220 package. If more power must be handled, then a larger package with smaller $R_{\Theta,jc}$ must be identified.

The most common heat sinks are made from aluminum. The smaller parts, like those shown in Figure 8.3 are stamped and then formed, while larger heat sinks are usually aluminum extrusions.

A problem frequently encountered in practice is that many semiconductor devices have their metal tabs connected to one of the device leads. For an N-channel FET, this is typically the drain (since from a thermal perspective, this offers the lowest thermal resistance from the junction to the case). Unfortunately in a buck chopper topology, the drain is connected to the input voltage and so the tab is electrically *live* with respect to the rest of the circuit. This prevents us from directly mounting the FET to the enclosure or from directly mounting it to a heat sink, as the enclosure or heat sink would pose an electrical hazard. The only way around this is to insert a spacer between the device and heat sink which has low electrical conductivity and good thermal properties as shown in Figure 8.5. Examples include mica, Sil-pads, Delta-pads, or Kapton.

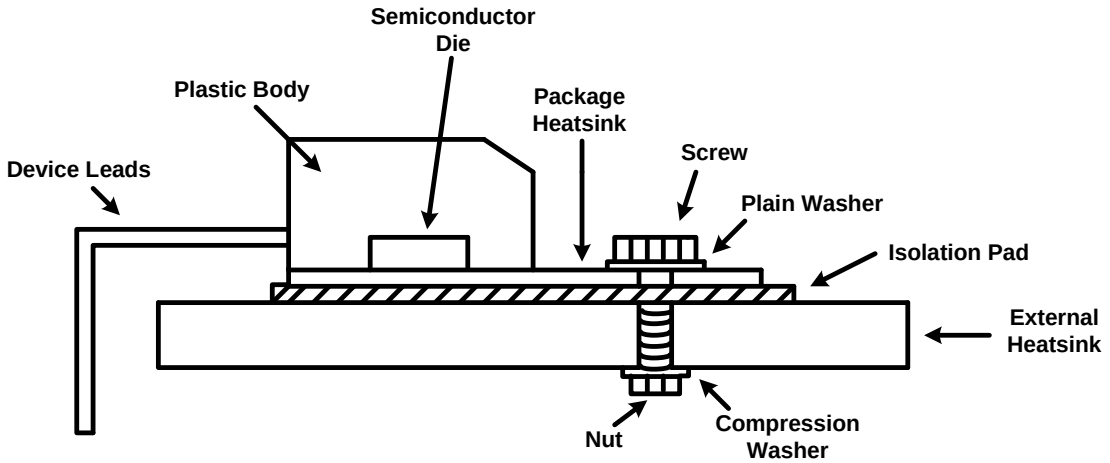


Figure 8.5: Illustration of the use of an Isolation Pad between the Case and Heat Sink

The question arises if electrical isolation is not an issue, why do we need anything in between the case and heat sink? To answer this, consider a microscopic view of the interface between the transistor case and the heat sink as shown in Figure 8.6. Note that the surfaces are far from smooth and that the air-pockets prevent good metal-to-metal contact. Silicon or thermal grease can fill these air pockets and provides a much lower thermal resistance than that of air.

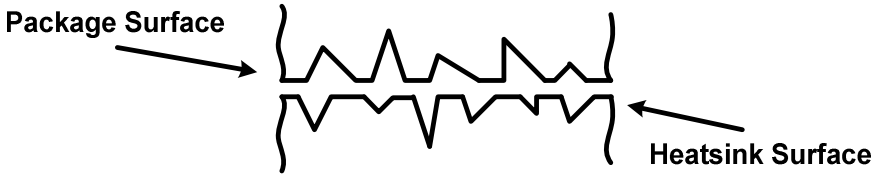


Figure 8.5: Microscopic View of the Junction between the Semiconductor Case and Heat Sink

Why is the phrase "if some is good, more is better!" wrong here? If we cake on the thermal grease, then we actually interfere with the best metal-to-metal contact points that exist between the case and heat sink and we increase the thermal resistance. Thus you want to minimize its application so that the thermal compound simply fills the gaps as shown in Figure 8.6.

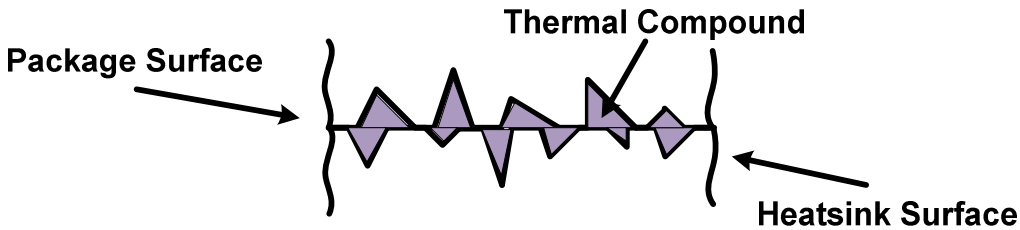


Figure 8.6: Illustration of Correct Application of Thermal Grease

The use of convective heat transfer enables you to use the same heat sink to handle a larger thermal heat load. The effective thermal resistance is lowered by incorporating a fan to transfer the heat to the moving air. Heat sink vendors provide curves that enable you to estimate the air flow required to reduce the heat sink thermal resistance to a given value. With this information, you can then size the appropriate fan. The cost that you pay is the efficiency penalty of having to now power a fan in addition to the buck chopper electronics. Size reduction can be gained if the fan is smaller than requiring a larger heat sink. That's enough heat management for now (for sure)!

Example 8.1: Let's compare two designs. Suppose we have a transistor part that has $T_{J,\max} = 175^{\circ}C$. It is being used in a buck chopper that supplies 500W at rated power. The switching frequency has been selected so that the total losses in the switch are 5% of the overall output power or 25W. The part is in a TO-220 package that has $R_{\Theta,JC} = 1.0^{\circ}C/W$ while the selected isolation pad has $R_{\Theta,CS} = 0.5^{\circ}C/W$. We do not want to operate the device at its maximum junction temperature but we wish to have a margin of $40^{\circ}C$. Now to the problem: determine the appropriate size of heat sink if the dc-dc converter maximum ambient temperature is $30^{\circ}C$ ($86^{\circ}F$) or $50^{\circ}C$ ($122^{\circ}F$).

We are essentially using (8.6) twice to perform this evaluation

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss}} - R_{\Theta,jc} - R_{\Theta,cs} = \frac{135^{\circ}C - 30^{\circ}C}{25W} - 1.0^{\circ}C/W - 0.5^{\circ}C/W = 2.7^{\circ}C/W$$

This would require the heat sink on the far left of Figure 8.3 where its $R_{\Theta,sa} = 2.6^{\circ}C/W$. If we consider our more extreme ambient condition

$$R_{\Theta,sa,\max} = \frac{T_{J,\max} - T_{A,\max}}{P_{diss}} - R_{\Theta,jc} - R_{\Theta,cs} = \frac{135^{\circ}C - 50^{\circ}C}{25W} - 1.0^{\circ}C/W - 0.5^{\circ}C/W = 1.9^{\circ}C/W$$

If we are limited to the heat sinks shown in Figure 8.3, we are in trouble. Our options are the following: (1) use a fan to lower the thermal resistance of the heat sink or (2) lower the losses by perhaps decreasing the switching frequency so the heat sink above can be used. Let's figure out how much we would need to reduce the losses

$$P_{diss} = \frac{T_{J,\max} - T_{A,\max}}{R_{\Theta,sa} + R_{\Theta,jc} + R_{\Theta,cs}} = \frac{135^{\circ}C - 50^{\circ}C}{2.6^{\circ}C/W + 1.0^{\circ}C/W + 0.5^{\circ}C/W} = 20.73W$$

Thus, we must reduce our switching losses by about 4.3W.

OK, so let's tie together our analysis of FET losses and FET data sheet characteristics with our thermal analysis. From Section 7, we found that we can model the FET on-resistance variation versus junction temperature by

$$R_{DS,ON} = \alpha \times R_{DS,ON}\Big|_{25^{\circ}C} \times \left(T_J - 25^{\circ}C\right) + R_{DS,ON}\Big|_{25^{\circ}C} \tag{8.11}$$

Where α is the slope of the normalized resistance versus temperature curve. This expression can be simplified to simply

$$R_{DS,ON} = m \times T_J + b \tag{8.12}$$

The FET conduction losses are then evaluated as

$$P_{FET,cond} = D \times I_{L,rms}^2 \times R_{DS,ON} = D \times I_{L,rms}^2 \times m \times T_J + D \times I_{L,rms}^2 \times b \tag{8.13}$$

snd the switching losses are known once the FET and driver are selected and will be a function of the switching frequency

$$P_{FET,SW} \approx \frac{1}{2} V_{in} \times f_{SW} \left(I_{L,\min} \times T_{SW,ON} + I_{L,\max} \times T_{SW,OFF} \right) = \beta \times f_{SW} \tag{8.14}$$

Let's next link these total losses into our presumed thermal model

$$T_J = \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa} \right) P_{diss} + T_A \tag{8.15}$$

To give the following expression

$$T_J = \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa} \right) \times \left(D \times I_{L,rms}^2 \times m \times T_J + D \times I_{L,rms}^2 \times b + \beta \times f_{SW} \right) + T_A \tag{8.16}$$

where we see that the junction temperature appears on both sides, so we can solve for it

$$T_J = \frac{T_A + \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}\right) \times \left(\beta \times f_{SW} + D \times I_{L,rms}^2 \times b\right)}{1 - \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}\right) \times \left(D \times I_{L,rms}^2 \times m\right)} \tag{8.17}$$

This "nasty" expression allows us to estimate the junction temperature given the thermal resistances of the FET, mounting, and heat sink. Let's try it out!

<u>Example 8.2:</u> Let's suppose that the FET on-state resistance is characterized by the following linear relationship with junction temperature $R_{DS,ON} = 0.004 \times T_J + 0.2$, the switching losses are characterized by $P_{FET,SW} \approx 1 \times 10^{-4} \times f_{SW}$, the desired inductor current waveform yields $I_{L,rms} = 4A$, the duty cycle is estimated at $D = 0.52$, and the thermal resistances are given by $R_{\Theta,JC} = 0.8^\circ C/W$, $R_{\Theta,CS} = 0.5^\circ C/W$, and $R_{\Theta,sa} = 3.7^\circ C/W$. Predict the actual junction temperature if $f_{SW} = 100kHz$ and $T_A = 25^\circ C$. Equation (8.17) gives

$$T_J = \frac{25^\circ C + \left(0.8 + 0.5 + 3.7\right)^\circ C/W \times \left(10W + 0.52 \times \left(4A\right)^2 \times 0.2\right)}{1 - \left(0.8 + 0.5 + 3.7\right)^\circ C/W \times \left(0.52 \times \left(4A\right)^2 \times 0.004\right)} = 100^\circ C$$

Let's contrast this with an "iterative" approach where we start by estimating T_J. Let's choose a temperature lower than what we found, say $80^\circ C$. This would lead to

$$R_{DS,ON} = 0.004 \times 80^\circ C + 0.2 = 0.52\Omega$$

The conduction losses are then computed as

$$P_{FET,cond} = D \times I_{L,rms}^2 \times R_{DS,ON} = 0.52 \times \left(4A\right)^2 \times 0.52\Omega = 4.33W$$

The total FET losses are then found by adding the switching and conduction losses

$$P_{FET,ave} = P_{FET,SW} + P_{FET,cond} = 10W + 4.33W = 14.33W$$

We can then finally compute the junction temperature given our thermal resistances and ambient temperature as

$$T_J = \left(R_{\Theta,jc} + R_{\Theta,cs} + R_{\Theta,sa}\right) P_{diss} + T_A = \left(0.8 + 0.5 + 3.7\right)^\circ C/W \times 14.33W + 25^\circ C = 96.7^\circ C$$

which is higher than our initial assumption of $T_J = 80^\circ C$. We could go back and use this new value to re-evaluate the on-state resistance, the conduction losses, and the junction temperature and find we are getting much closer.