9.0 Pulse-Width Modulation

In a buck chopper, we require a stream of pulses to go to the high-side driver in order to initiate turning ON and OFF the main FET. Further, the duty cycle of the pulse stream, or ratio of switch ON time to switching period, must be adjustable so that the output voltage can be well regulated in the presence of changes in input voltage and output load or parameter variation due to temperature or ageing. The duty cycle will also need to be varied in order to improve the dynamic response, say during step changes in the output load, to avoid large output voltage overshoots and long settling times. The Pulse-Width Modulation, or PWM, device must be able to at a minimum (1) generate the required switching frequency; (2) properly interface with the high-side driver, providing a suitable ON and OFF voltage level; and (3) enable convenient adjustment of the duty cycle.

Our first experience with PWM was with the 555 timer configured in astable multi-vibrator mode. This circuit is shown in Figure 9.1.

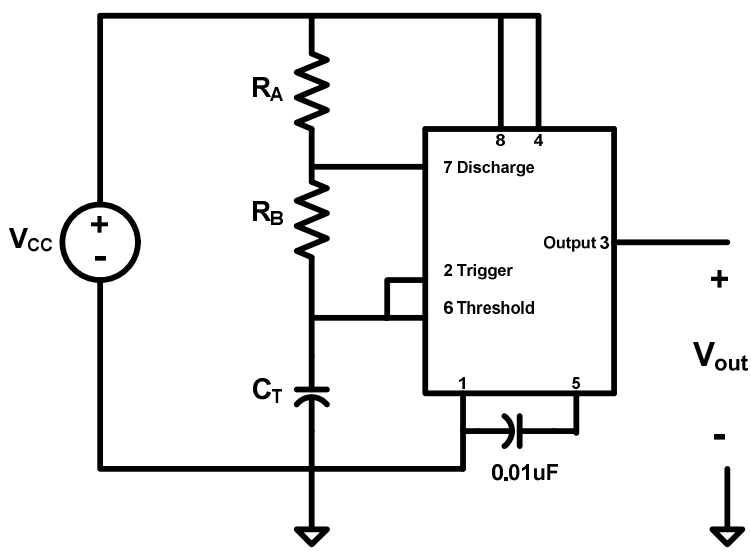

Figure 9.1: Astable Multivibrator 555 Circuit

This circuit operates by periodically charging and discharging capacitor C_T. The switching threshold levels are set internally at $V_{CC}/3$ and $2V_{CC}/3$. When the power supply is turned ON, the capacitor is charged through R_A and R_B up to a level of $2V_{CC}/3$. This then activates an internal transistor which brings the discharge terminal down to near zero volts, allowing the capacitor to discharge through R_B. Once the capacitor voltage drops to $V_{CC}/3$ the internal transistor turns OFF and the discharge terminal appears as an open circuit. The capacitor returns to charging. The oscillation frequency is governed by

$$f = \frac{1.44}{\left(R_A + 2R_B\right)C_T} \tag{9.1}$$

while the duty cycle is given by

$$D = \frac{R_A + R_B}{R_A + 2R_B} \tag{9.2}$$

Upon closer inspection of (9.2), the duty cycle can be adjusted between 0.5 and 1 by varying the resistors. An alternative to this is shown in Figure 9.2 where we have replaced the two separate resistors by a potentiometer (here, arbitrarily drawn as a $10k\Omega$ value) and have inserted a diode between the Discharge and Threshold terminals. The diode essentially steers the capacitor charging current so it only goes through the R_1 portion of the potentiometer. The capacitor then discharges only through the R_2 portion of the potentiometer. The frequency and duty cycle equations are modified to

$$f = \frac{1.44}{R_{Pot}C_T} \tag{9.3}$$

$$D = \frac{R_1}{R_{Pot}} \tag{9.4}$$

Once R_{Pot} is selected, C_T will fix the oscillation frequency and the portion of the potentiometer resistance R_1 dictates the duty cycle.

The “idealized” output waveforms of the circuit are illustrated in Figure 9.3. The LM555 data sheet shows that the output pin of the chip can source or sink up to 200mA, the power supply voltage can be anywhere between 4.5V and 18V, the chip will draw about 6-15mA of supply current, the output “low” voltage will be somewhere between 0-2V depending on load current, and the output “high” voltage will be 1 to 2V less than the supply voltage.

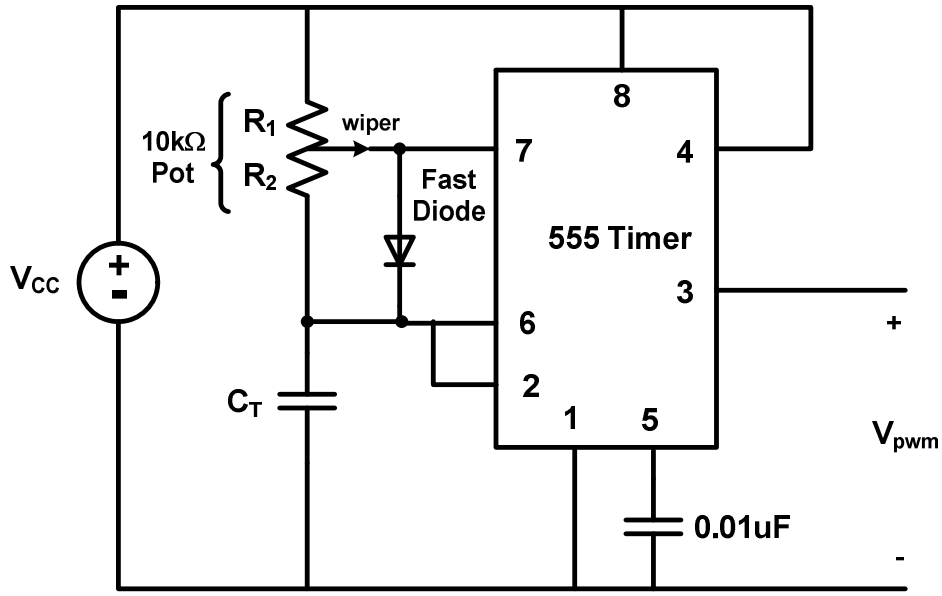

Figure 9.2: Astable Multivibrator with Manually Adjustable Duty Cycle

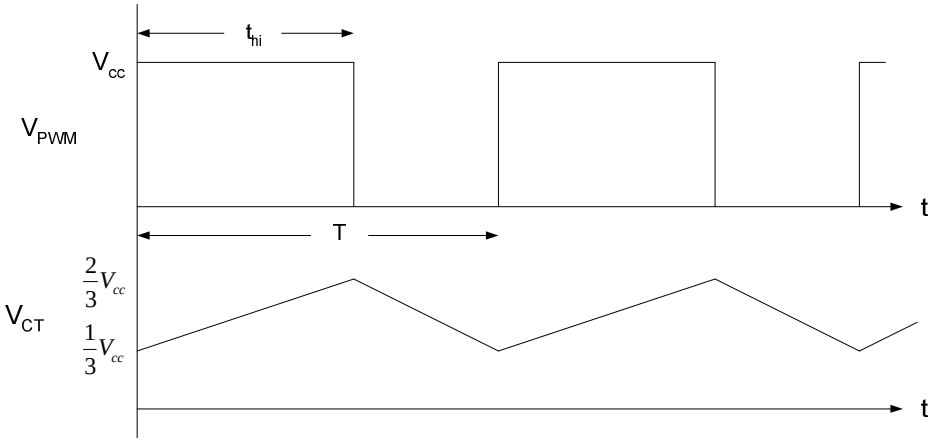

Figure 9.3: Idealized Astable Multivibrator Output Waveforms

The disadvantage of this circuit for use in a DC-DC buck chopper is that the duty cycle must be *manually* controlled via adjustment of the potentiometer. For a buck chopper, we will find in the steady state that the duty cycle must be continuously tweaked to take into account operation at different input voltages and output loads and for changes in parameters due to temperature. Further during transient events (i.e. switching in additional loads), it will be necessary to dampen the response by dynamically controlling the duty cycle to avoid large overshoots, oscillations, and long settling times.

We can implement a dynamic control of the duty cycle by using the "Control Voltage" or terminal pin 5 of the 555 timer. The control voltage essentially enables the user to reset the upper threshold voltage from $2V_{CC}/3$ to the external value. The problem with this approach is that the switching frequency is simultaneously effected.

Example 9.1: We would like to design a 555 timer circuit to interface with the IR2117 high-side driver and deliver a PWM signal at 80kHz. Assume that you have a $10k\Omega$ potentiometer available.

Using (9.3),

$$C_T = \frac{1.44}{R_{Pot} \times f} = \frac{1.44}{10k\Omega \times 80kHz} = 1.8nF$$

If we use a 2nF capacitor, the theoretical frequency drops to 72kHz; however, equation (9.3) is approximate so trial and error might be required to assess the effect. Now we must also consider the power supply requirement for the 555 chip. The IR2117 driver requires a power supply voltage greater than 9.6V (from Table 5.1). Also, we are told that the 555 output voltage may be 1 to 2V below its supply voltage. Thus to be safe, we probably want a supply voltage at least $V_{CC} > 10V + 2V = 12V$.

An alternative solution is to use a specially-designed PWM chip, such as the TL5001 produced by Texas Instruments. In addition to conveniently setting up an oscillation frequency and enabling duty cycle control, this chip provides an amplifier that can be used to implement the buck chopper feedback control and a convenient voltage reference. The pin out for this chip is shown in Figure 9.4.

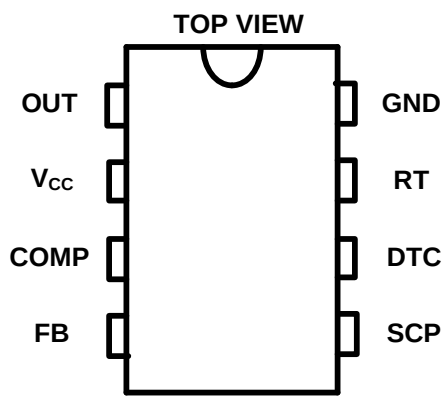

Figure 9.4: TL5001 PWM Chip Pin Out

First there is an important distinction between the 555 timer and the TL5001. The TL5001 has an open-collector output, meaning that the output terminal is internally connected to the collector of a transistor. So the output voltage will not naturally transition between zero and V_{CC} and the terminal can only sink current, not supply any. With that said, let's briefly review the various terminal pins. Obviously V_{CC} is the power supply voltage and the data sheet lists that it must be between 3.6V and 40V. The oscillator frequency can be set between 20kHz and 500kHz by connecting a resistor between terminal RT and GND (ground). Acceptable resistor values range between $15k\Omega$ and $250k\Omega$ as shown in Figure 9.5.

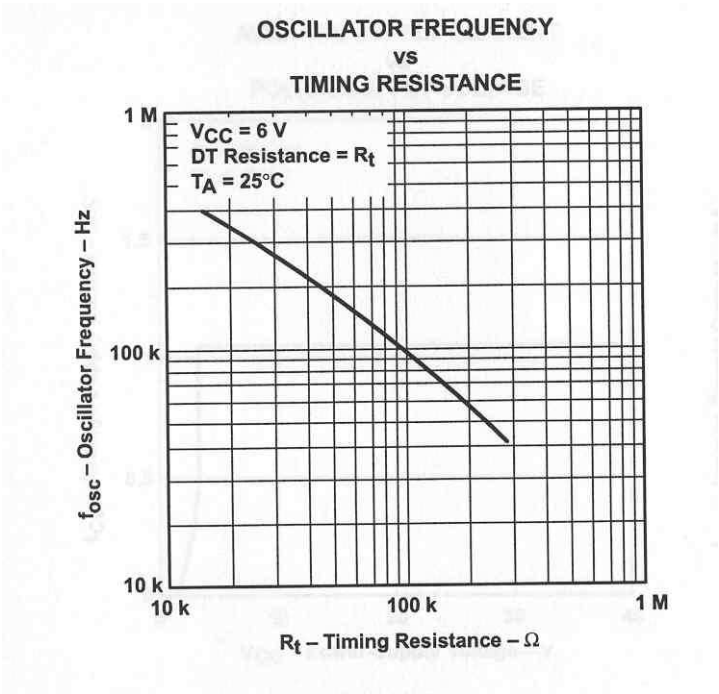

Figure 9.5: Timing Resistance versus Oscillator Frequency

The FB terminal of the TL5001 goes to the inverting input of an error amplifier as shown in the functional block diagram in Figure 9.6. Typically it will be connected to an external compensation network leading back to the output of the buck chopper. The COMP terminal connects to the output of this amplifier, enabling the designer to “close the loop” around the amplifier. The COMP terminal goes directly to the PWM comparator. An internally-derived 1V reference signal is applied to the non-inverting terminal of the error amplifier. This will essentially act as a scaled version of the desired output voltage.

The internal oscillator output is a triangular wave varying between 0.7V and 1.3V (output of box labeled OSC in Figure 9.6). A comparator compares the triangular wave signal to the combination of the error amplifier output and the signal at the DTC terminal. DTC stands for “Dead Time Control” and this terminal provides a means for limiting the output duty cycle to some value less than 100% by establishing a voltage at DTC between 0.7V and 1.3V (details available in the data sheet). In open-loop operation, varying the COMP terminal signal between 0.7V and 1.3V will provide the means to vary the duty cycle between 0 and 100%.

The SCP terminal stands for “Short Circuit Protection.” It essentially provides the capability to disable the PWM chip when a short circuit occurs at the output of the DC-DC converter. This will force the converter switch to be OFF and stay OFF until the short circuit is cleared (more details are available in the data sheet).

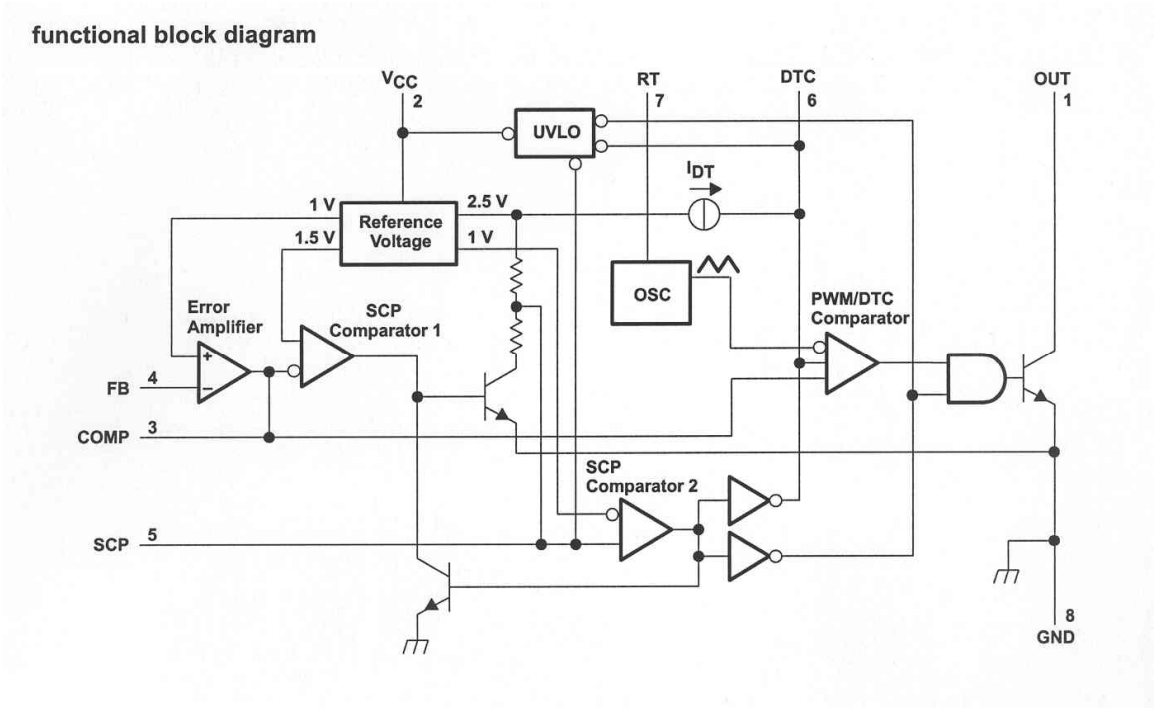

Figure 9.6: Functional Block Diagram of TL5001 PWM Chip

The OUT terminal shown in Figure 9.6 is an open-collector transistor with a maximum current rating of 21mA and a voltage rating of 51V. The voltage between this pin and ground will depend on the sinking current as shown in Figure 9.7 and the state of the PWM/DTC Comparator. If the transistor is OFF, then the terminal will appear as an open circuit. If the transistor is ON and 5mA is made to flow into the collector for example, then the voltage at OUT will be about 1.1V. A composite circuit diagram including the TL5001, a high-side driver, and the buck chopper is shown in Figure 9.8. The pull-up resistor R_{PU} is sized to set the sink current of the open-collector transistor according to

$$I_{Sink} \approx \frac{V_{DR}}{R_{PU}} \tag{9.5}$$

Note, an actual buck converter circuit would also utilize a compensation network connected from the converter output back to terminals FB and COMP of the TL5001. Discussion of the analysis and design of such a network is beyond the scope of this writeup.

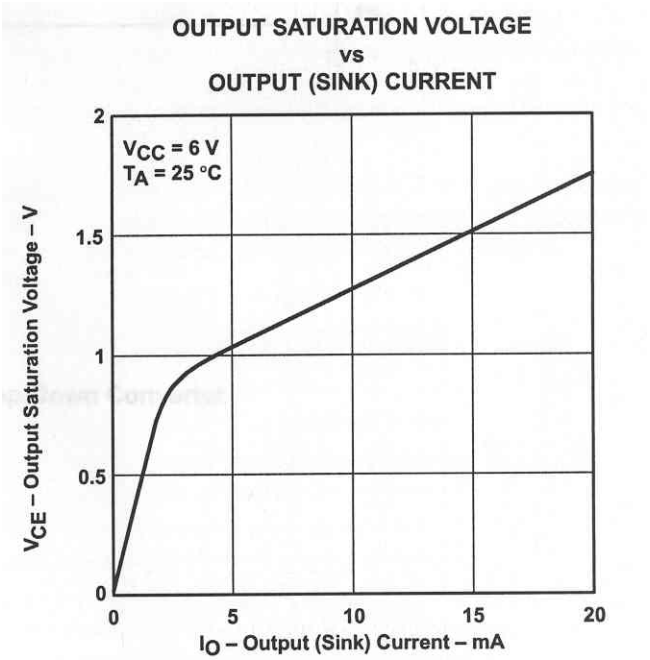

Figure 9.7: Output Sink Current versus Output Voltage

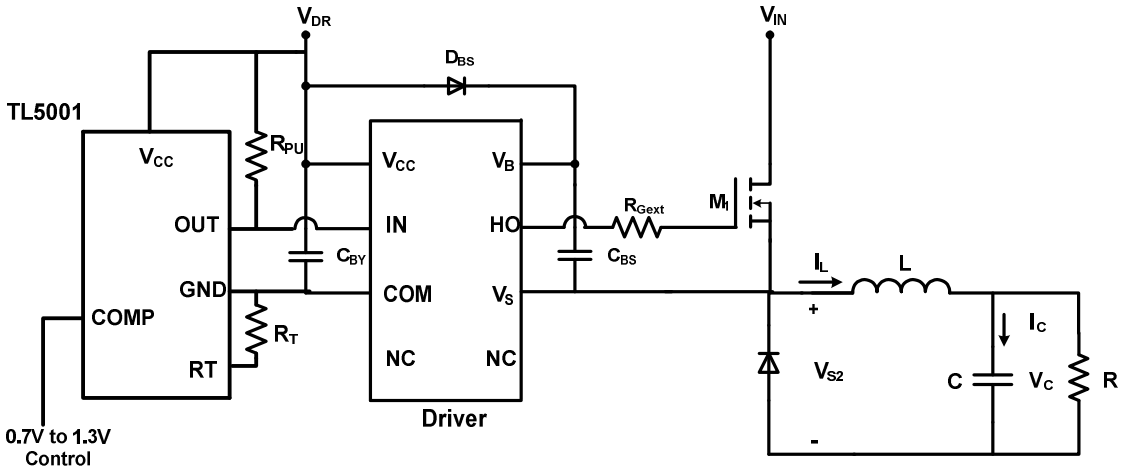

Figure 9.8: TL5001 Connected to a High-Side Driver and Buck Chopper

Many different PWM chips exist. You can search for instance at digikey under Integrated Circuits and then Voltage Regulators – PWMs. Table 9.1 contains some common choices. Note it is key to identify the frequency capability of the chip, the maximum duty cycle, and the type of output (how this chip will interface to a high-side driver or other option). In addition it is also important to recognize that PWM chips are available in what is called voltage-mode and current-mode. These terms refer to how the buck chopper is to be controlled and is an excellent future topic for study!

Table 9.1: Commonly Available PWM Chips (in DIP Packages)

Component	$f_{\max}$	C_T Req.	Outputs	$D_{\max}$
TL494	300kHz	Yes	2 (common emitter or emitter follower)	45%
UC3525	400KHz	Yes	2 (totem pole)	50%
UC3823	1MHz	Yes	1 (totem pole)	80%
UC3573	300kHz	Yes	1 (to gate driver)	96%
UC3824	1MHz	Yes	2 (totem pole)	100%
UCC35705	4MHz	Yes	1 (to gate driver)	93%

Example 9.2: Using the TL5001 PWM chip, design an output that has a frequency of 100kHz and where the PWM low signal will be less than 1V. Assume that the gate drive voltage is set at 12V to interface with the IR2117 gate driver. Specify values for R_T and R_{PU}.

The starting point is Figure 9.5 where we see that at 100kHz, the timing resistor must be approximately $100k\Omega$. To satisfy the output voltage being less than 1V when the chip is sinking current, we use Figure 9.7 to observe that 1V requires the sinking current to be about 4mA. We can then use equation (9.5) to solve for the pull-up resistor

$$R_{PU} \approx \frac{V_{DR}}{I_{Sink}} = \frac{12V}{4mA} = 3k\Omega$$

If this is not available, then either a $2.7k\Omega$ or $3.3k\Omega$ resistor ought to be adequate.