

EE334 PRACTICAL EXERCISE: A-to-D & D-to-A Conversion

Team Name: _____ Section: _____ Date: _____

I. Goals:

- a. Develop familiarity with analog-to-digital converters.
- b. Implement the circuits necessary to complete a 2-bit analog-to-digital conversion.
- c. Interface a circuit designed on a quad board with a circuit programmed in an Altera DE-1 Board.
- d. Develop familiarity with digital-to-analog converters.
- e. Implement the circuits necessary to complete a 2-bit digital-to-analog conversion.
- f. Compare the original analog signal to a signal that has gone through an ADC and a DAC.
- g. Encourage working in teams and task organization.

II. Objective:

- a. Build a working 2-bit analog-to-digital converter.
- b. Design and build a 3 to 2 bit encoder.
- c. Build a working 2-bit digital-to-analog converter.

III. Equipment:

- a. Resistor: 10k Ω (4 ea), 2k Ω (4 ea)
- b. 1 IDE Cable
- c. Op-Amps: 741 (4 ea)
- d. Altera DE-1 Board with laptop
- e. Quad board with wires
- f. Alligator clip wires (6 ea)

IV. Organization:

- a. Each team will consist of 3 groups. Group One will build and test the ADC, Group two will build the Encoder using Quartus II and the Altera DE-1 Board, and Group Three will build and test the DAC.

Group One : _____

Group Two: _____

Group Three: _____

Analog-to-Digital Converter

V. **Group 1:** Design A-to-D: TASK: *Produce outputs I_2 , I_1 , and I_0 from a 2 bit Flash ADC.*

- a. As discussed in class, a flash ADC consists of major components: an analog voltage input, a resistor network, a set of op-amps functioning as comparators, an encoder to change the outputs of the comparators into a binary number, and a display device for the binary output. See the block diagram in Figure 1 below. In the exercise, the DC voltage supply will be the analog input, the quad board will contain the resistor network and the set of op-amps, and the Altera DE-1 Board built by Group Two is the encoder and the digital display.

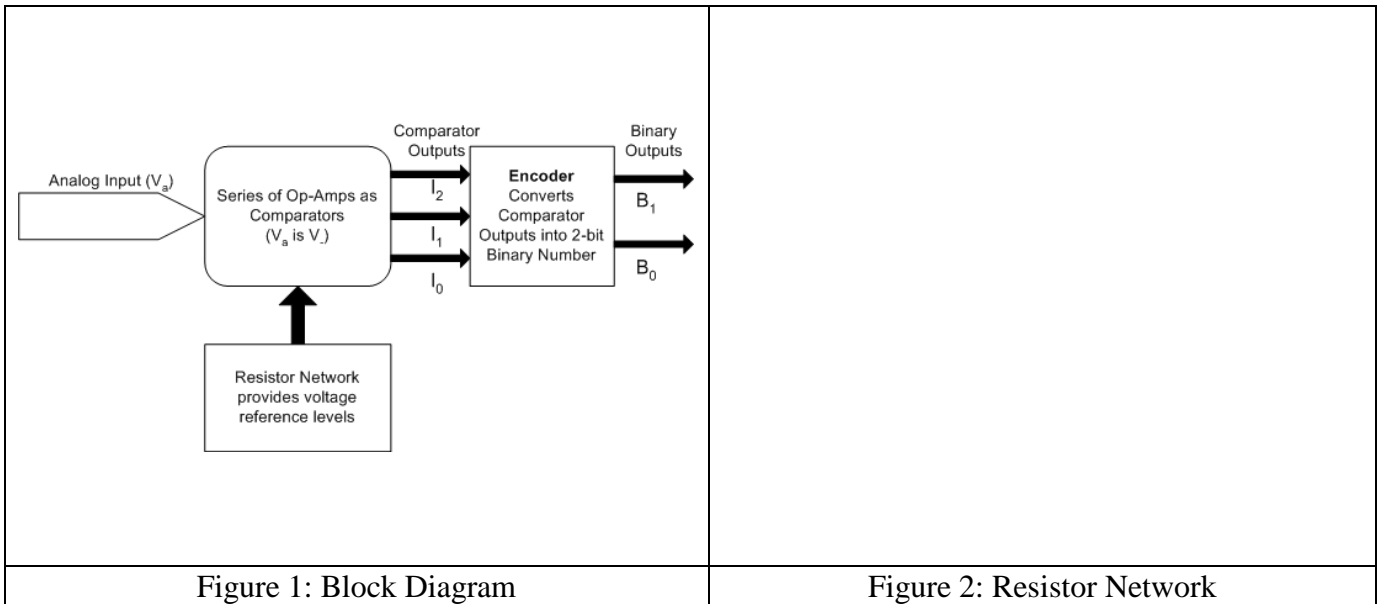


Figure 1: Block Diagram

Figure 2: Resistor Network

- b. Design the resistor network and the set of op-amps needed using the $2\text{ k}\Omega$ resistors and the 12 V DC supply of the left side of the lab bench. Your three comparators should have 3V, 6V, and 9V into the V_- input. **Draw your resistor network including the comparators in Figure 2.** Tie your analog input into the V_+ of each op-amp.
- c. The desired output of the comparators is +5V for Logic HIGH and 0V for Logic LOW. Since the 741 OP AMP is not designed to function as a comparator, the rail voltages ($+V_{CC}$, $-V_{CC}$) must be adjusted to the following approximate values: $+V_{CC} = +6.11\text{ V}$
 $-V_{CC} = -1.89\text{ V}$
- d. After building the circuit, test the output using the DC Power Supply. Verify your results and record them below.

Analog Input	I_2 I_1 I_0	Analog Input	I_2 I_1 I_0
0 V		7 V	
2 V		8 V	
4 V		10 V	
5 V		11 V	

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Encoder using Altera DE-1 Board

VI. **Group 2:** **Design Encoder:** TASK: Use outputs I_2 , I_1 , and I_0 from a 2 bit Flash ADC and encode them into 2 bit binary output using Altera DE-1 Board. Produce outputs B_1 and B_0 .

- a. Group 1 will be producing outputs 000, 001, 011 and 111 that need to be mapped into the desired 2-bit binary outputs (00, 01, 10, and 11 respectively). You are to design an encoder to change the outputs of the comparators into a binary number. You will also connect the outputs B_1 and B_0 to the 7447 and display device the BCD equivalent of the output. Fill in Table 1 with your desired output and use a K-Map to derive the Minimum SOP expressions for the binary outputs (B_1 and B_0). There will be several Don't Care Outputs.

K – Maps for B_1 and B_0

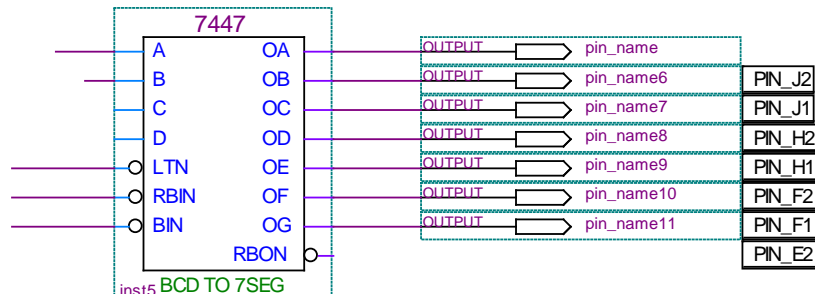
Output of Comparators			Desired 2-bit binary output	
I_2	I_1	I_0	B_1	B_0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Table 1

$B_1 =$ _____

$B_0 =$ _____

- b. Build the circuit in Quartus II using the Boolean expressions found in part a. You will have 3 external inputs, I_2 , I_1 and I_0 and two outputs, B_1 and B_0 . **Use the pin assignments for Expansion Header 1 as described in Figure 5 and shown in Figure 4.** Also, route the Outputs B_1 and B_0 into the 7447 and display the output on the 7 segment display (Use Output Pin Assignments as in diagram below).



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- c. Before you energize the circuit, connect an alligator clip from the Altera board's reference to the ground on the lab bench PIN '12' on Expansion Header 1. Test your circuit using Power supply to simulate I_2 , I_1 and I_0 and verify you are producing the required output.



Figure 3: IDE Cable – See instructor and/or Lab tech for help hooking this up to Altera DE-1 Board

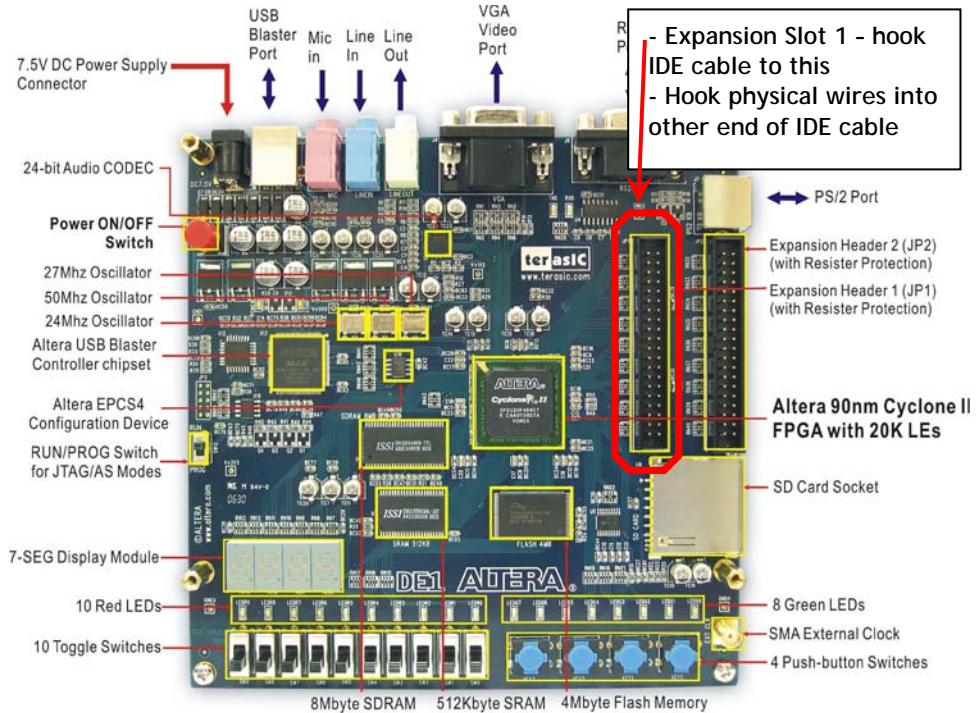


Figure 4: Altera Connection

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Digital-to-Analog Converter

VII. **Group 3:** Design D-to-A: TASK *Use outputs B_1 and B_0 produced by Group 2 and convert them to an analog signal.*

- a. As discussed in class, an inverting summing amplifier can be used as a simple digital-to-analog converter. Using one op-amp and the $10k\Omega$ resistors, design a DAC that has a gain of 2 (ie $R_f = 2 \times$ value of MSB Resistor). Use the +12 V DC supply for $+V_{CC}$ and the -12 V DC supply for $-V_{CC}$. Draw your circuit in Figure 6.
- b. Based on the design of your DAC, complete the expected values in Table 3.



Figure 6: Inverting Summing Amplifier

Binary Input		Analog Output
B_1	B_0	V_{out}
0	0	
0	1	
1	0	
1	1	

Table 3

- c. The input for your DAC will be the binary output from the 2-bit flash ADC that Groups 1 and 2 built. Test your DAC by simulating receiving binary inputs of 3.5V and 0V for B_1 and B_0 and record your values in Table 4. Note: The Altera outputs a value of 3.5 Volts for a logical 1 and 0 Volts for a logical 0.

B_1	B_0	V_{out}
0V	0V	
0V	3.5V	
3.5V	0V	
3.5V	3.5V	

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Combining the Circuit

VIII. Construct 2-bit ADC / DAC: TASK Combine each of the designs of the 3 groups.

- a. After each group has verified their results and your instructor has signed off, combine the 3 designs as shown in Figure 7. The goal is to input an analog signal and compare this signal using an OScope with the digitized version.
 1. Generate the AC analog input using the function generator with the following settings: 10 V_{PP} with a 5 V DC offset, f = 1 kHz. (Make sure in Output = HighZ)
- b. Connect the original analog input to the o-scope into Ch. 1. Connect the digitized analog signal (i.e. output of the DAC) to Ch.2. Don't forget to refer the o-scope to ground.

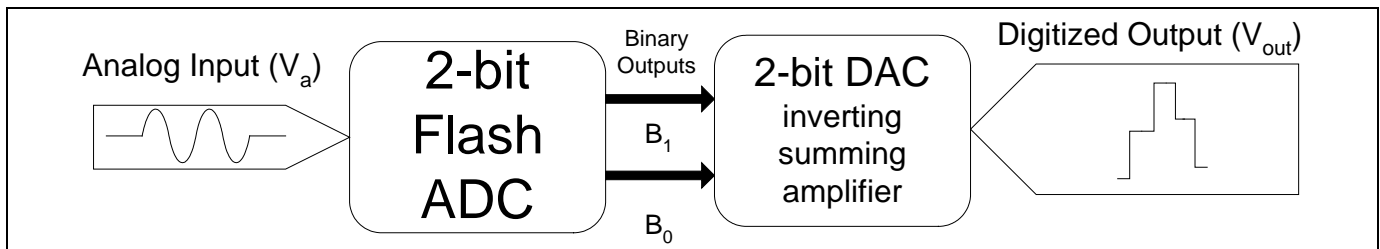


Figure 7: Block Diagram

- c. Adjust the o-scope to the following settings:
 1. Invert Ch. 2
 2. Select Edge Triggering (↑). Adjust the trigger level until the signals freeze.
 3. Adjust the V/div scale so both signals appear to have the same magnitude.
 4. Adjust the sec/div scale to display to full cycles.
- d. **Results** Sketch the result of the conversions from the o-scope below in Figure 7. Make sure you show the differences between the original and digitized signal.



Figure 7

- e. Increase the frequency of the input signal to 10 kHz. Describe what happened to the digitized signal. Explain the result.