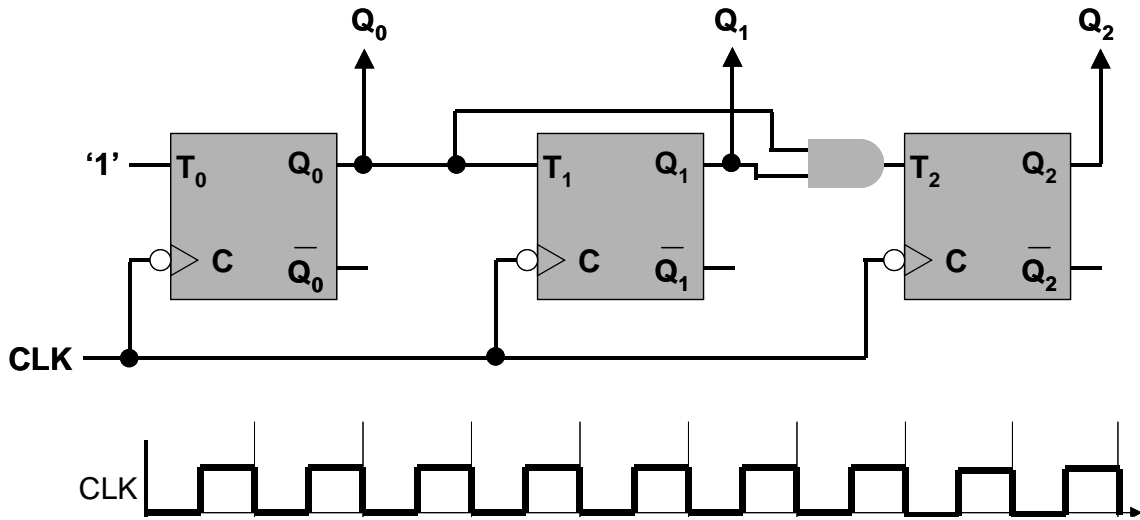


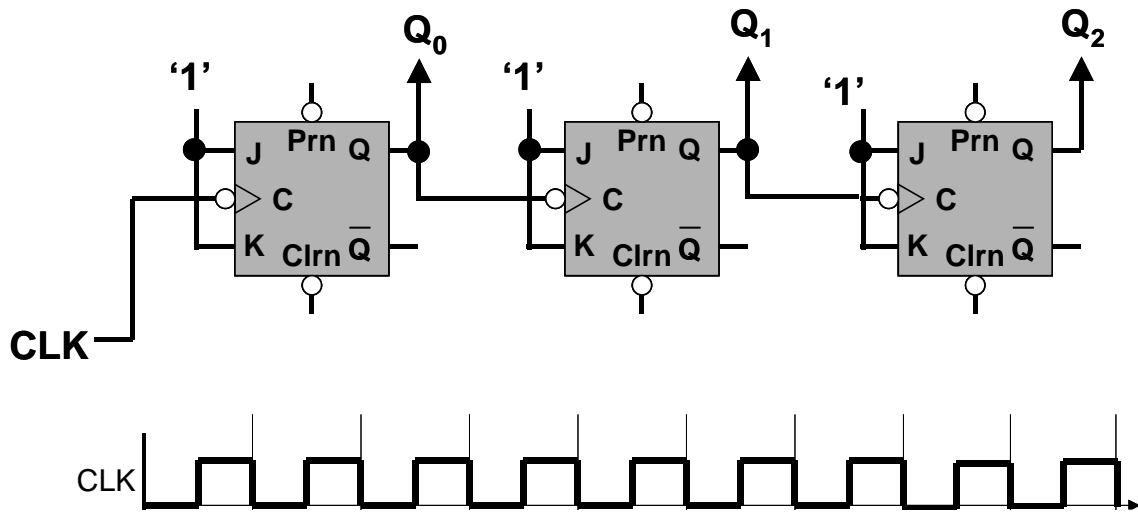
3. The circuit in Figure 1 is **synchronous**. The circuit in Figure 2 is **asynchronous**. What causes one circuit to be asynchronous and the other synchronous?

4. Complete a timing diagram for the circuit of Figure 1. The circuit is shown again for your convenience. Assume the Q values start low.



5. Between each falling clock the Q values are stable. For each stable period, list the Q values in the order Q₂Q₁Q₀. What pattern is created by the Q values?

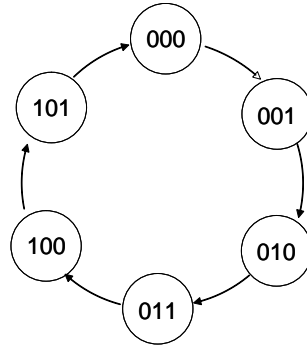
6. Complete a timing diagram for the circuit of Figure 2. The circuit is shown again for your convenience. Assume the Q values start low.



7. Between each falling clock the Q values are stable. For each stable period, list the Q values in the order $Q_2Q_1Q_0$. What is the pattern of the Q values?
8. Was it easier or harder to complete the timing diagram for the circuit of Figure 1 than for Figure 2? Why?

The circuits in Figures 1 and 2 are examples of circuits that count. More specifically they are what are called **mod-8 up counters**. The “mod-8” refers to the fact that they go through 8 states (the numbers 0 through 7) and then repeat. “Up” is the direction of the counting. More specifically, the circuit in Figure 1 is a *synchronous mod-8 up counter* while the circuit in Figure 2 is an *asynchronous mod-8 up counter*.

When designing counters, or other sequential devices that need to repeat states, a useful tool is the **state diagram**. A state diagram shows how the machine should move from one state to another. Here’s the state diagram for a mod-6 up counter.

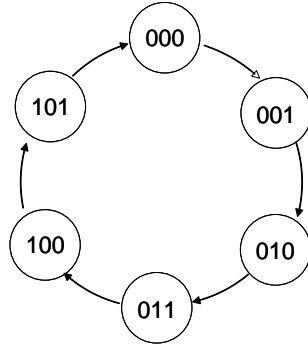


9. Draw a state diagram for a mod-3 up counter.

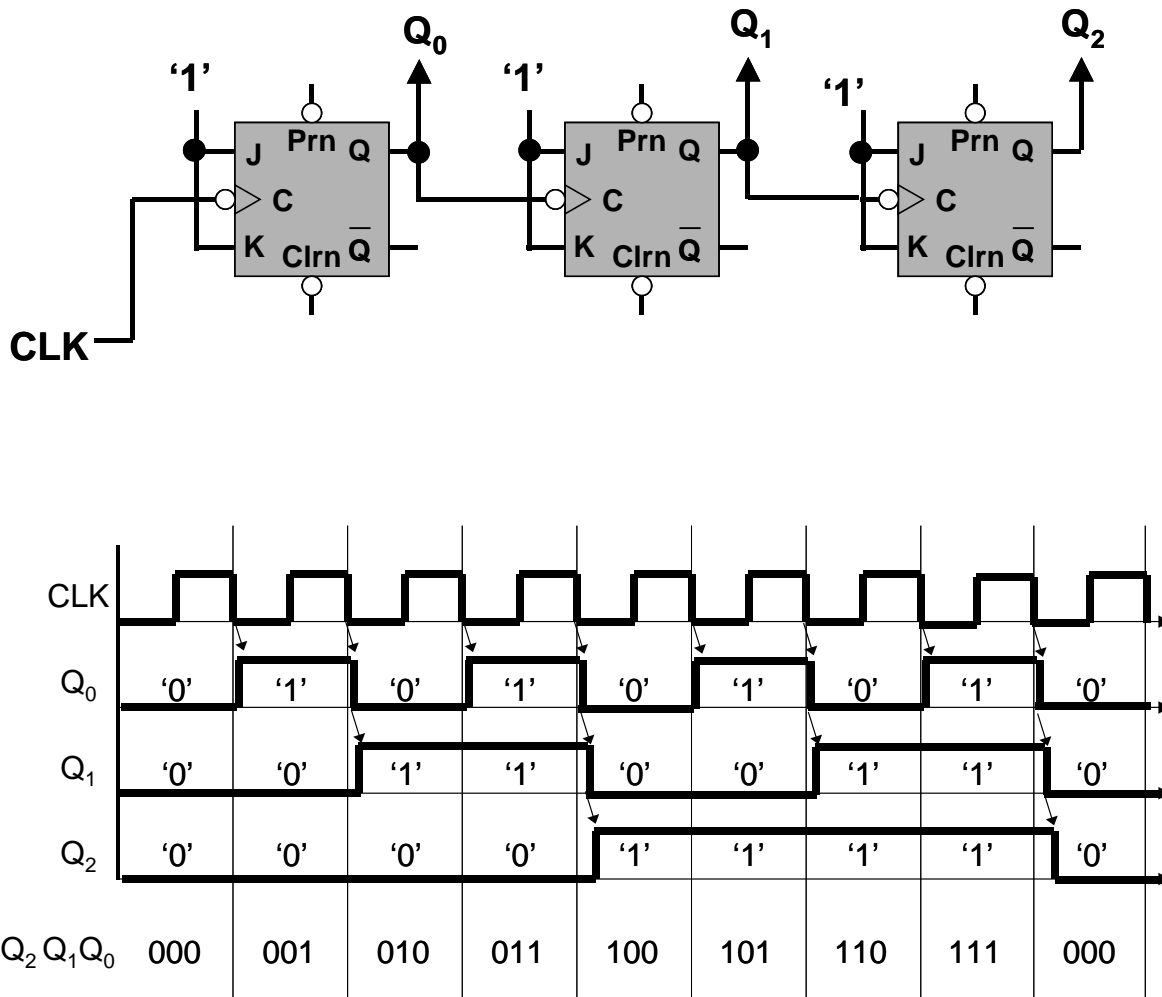
10. Draw a state diagram for a mod-4 down counter.

11. Draw a state diagram for a mod-5 up counter that starts at 010 and goes to 110 before repeating.

EE 334
Counters



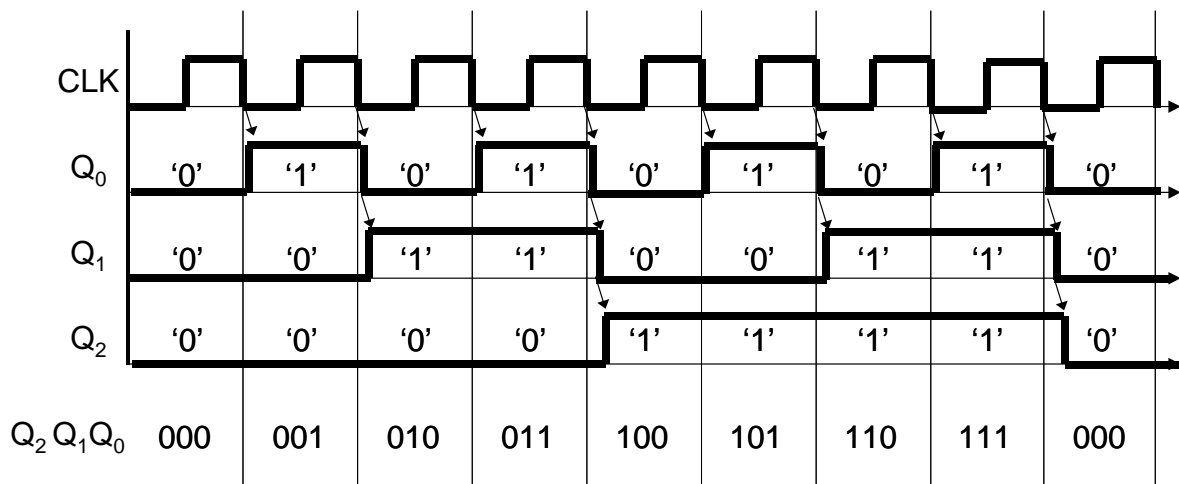
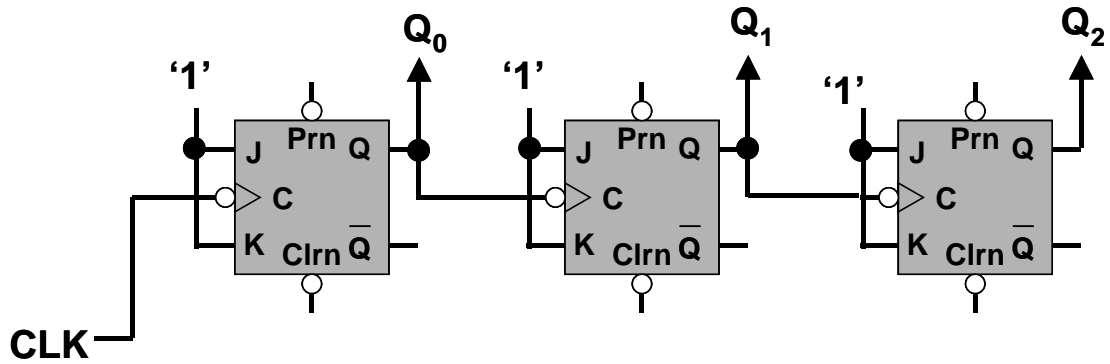
12. Repeated above is the state diagram for a mod-6 up counter. The counter has how many bits?
13. What bit patterns are missing?
14. When building sequential logic devices, we have to pay attention to any missing bit patterns. Any guesses as to why?
15. Modify the mod-6 counter above to account for the missing states.



Shown above is the asynchronous mod-8 up counter of Figure 2 along with its corresponding timing diagram.

16. Draw a state diagram for a mod-5 up counter.

17. Turn the counter into a mod-5 up counter by adding some external logic. The logic should sense one or more of the Q values and then cause each flip-flop to reset to 0. Note: state "100" should last for its full duration. Feel free to draw on the circuit diagram above.



18. Now turn the counter into a mod-6 up counter by adding some external logic.
19. Describe a potential problem with the modifications you made to the mod-8 counter in problems 17 and 18? Hint: think about disastrous consequences.
20. We built counters using flip-flops. Flip-flops are simple memory devices. What is it about counting that requires the use of memory devices?

Next time: How to design counters or any state machine using flip-flops.