EE342 LAB 1 BJT DESIGN

Design a 2-stage amplifier using 2N3251 transistors to provide the following:

Input: .1Vp-p sinusoid (source resistance = 50Ω)

Output: 1st stage: .5Vp-p sinusoid (+/- 5 %) (180° out of phase with input)
2nd stage: 2Vp-p sinusoid (+/- 5 %) (in phase with input)

Constraints: 1. Use -15V DC supply
2. Design so that 5kHz is well within mid-band region.
3. Specified output signal amplitudes should be stable in mid-band region.
4. The input resistance of the amplifier >10kΩ and be able to provide its output to a 2kΩ load.
5. The output should have zero Volts DC.
6. The DC operating points are to be chosen by the designer, but make sure your choices allow for linear operation.

Provide a preliminary design with resistor values and all calculations shown. Simulations on PSPICE may be provided as well, but the theoretical work and assumptions to arrive at your particular design must be included (both DC and AC analysis).

In Lab, you must demonstrate your design results to the instructor, make sure to indicate any changes of resistor and capacitor values from the preliminary design to meet the requirements of the gain or frequency range. You should document your design's bandwidth, by providing a table of your measured data and use that data to provide a dB vs log frequency plot of your gain. Submit this and all design calculations and simulations in a formal lab report. (Scope data is also nice to include in report) Example of table:

f(Hz)	vin(p-p)	vo2(p-p)	dB gain (=20 log | vo2 / vin|)
50			
100			
1K			
5K			
7K			
10K			
20K			
50K			
100K			
500K			
1M			