

Device	Starting address
768 bytes of high-speed (15 ns) static RAM	0x0400
Four ACIAs	0x1000
One PIA	0x1010
Three buffers	0x1020
2K ROM	0x2800

Table 1: Desired System Configuration

Device	Architecture	Chip-Select Labels
2K RAM (low-speed)	2048×8 bits	CS ₀ , CS ₁ , CS ₂
4K ROM	4096×8 bits	OE ₁ , $\overline{\text{OE}}_2$
MC6820 PIA (Parallel I/O)	4×8 bits	CS ₀ , $\overline{\text{CS}}_1$, $\overline{\text{CS}}_2$
MC6850 ACIA (Serial I/O)	2×8 bits	CS ₀ , $\overline{\text{CS}}_1$, $\overline{\text{CS}}_2$
Octal buffer	1×8 bits	G ₀ , $\overline{\text{G}}_1$
High-speed RAM	256×8 bits	$\overline{\text{CS}}_0$, $\overline{\text{CS}}_1$
16K ROM	16,384×8 bits	$\overline{\text{OE}}$
74LS165 Parallel-load 8-bit shift reg	1×8 bits	$\overline{\text{LD}}$
4K low-speed RAM	4096×8 bits	$\overline{\text{OE}}_1$

Table 2: Available Devices