

EE361 Microcomputer-Based Digital Design

Quiz 4 Solution

OPEN BOOK, OPEN NOTES.

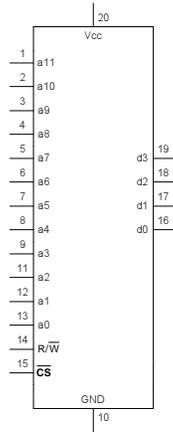
Name: _____

Section: _____

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There is another problem on the back of this sheet.

1. Consider this memory integrated circuit:



- a. How many distinct locations are there within this chip?

SOLUTION

There are 12 address lines, so the chip has $2^{12} = 4096$ distinct locations.

- b. How many bits are stored at each location?

SOLUTION

There are four data lines, so each word must store four bits.

- c. How many bits of data can this chip store?

SOLUTION

The number of bits is the product of the number of locations and the number of bits in each location:

$$\begin{aligned} n &= (4096 \text{ locations}) \left(\frac{4 \text{ bits}}{\text{location}} \right) \\ &= 16384 \text{ bits.} \end{aligned}$$

2. Suppose a certain PIC16F884 is configured to operate with a 15 MHz crystal oscillator. The SSPCON register contains the hexadecimal value 32_{16} . During those times when data are actually being transmitted by the processor, what is the throughput in useful bits per second? (A useful bit is a data bit, as opposed to an overhead bit. Assume parity bits are not being used.)

SOLUTION

Bit 5 of the SSPCON register is the SSPEN bit. Here, it has the value 1, so the synchronous port is enabled.

The bits of SSPCON that govern the mode of the synchronous serial port are SSPM<3:0>, which in this problem correspond to the low-order bits in 32_{16} , that is, $2 = 0010_2$. This forces the SPI Master Clock mode with a clock rate $f_{\text{SPI}} = \frac{f_{\text{osc}}}{64} = 234\,375$ Hz. The SPI Master Mode waveform in Figure 13-2 on page 185 of the datasheet shows that there is no overhead: every bit period is used to transmit a data bit. There are no overhead bits. Therefore, the throughput is 234 375 Hz.