United States Naval Academy

Electrical Engineering Department

EE361 Test 2 Solution

30 October 2008

1. Do a page check now. You should have one title page and nine pages of problems, totalling 10 pages in all. *Please do not remove staples from the examination booklet.*

2. Show all work to receive maximum partial credit.

3. Work neatly and strive for clarity. Unclear answers earn little credit (if any).

4. You may use any calculator you have brought with you. You may not borrow a calculator from anyone during the exam. Although you may also use the computer at your seat, you may *not* make use of e-mail, chat, instant messenger, or any other program or device allowing one-way or two-way communications with other people, whether classmates or not.

5. If you make any assumptions necessary to proceeding, state them clearly.

6. *Do not discuss this test with anyone until it has been handed back to you after grading is complete.*

7. Each problem is worth the following points:

Problem	Points	Score	Problem	Points	Score
1	20		4	8	
2	32		5	4	
3	16		6	4	
			Total:	**84**	

8. You have 1 hour 50 minutes to complete the test.

9. Upon the command of your instructor, you may commence work. Good Luck!

Name: _____

Section: _____

Date: 30 October 2008

1. (20 pts) For the following questions assume you are using a PIC16F884 running with a crystal oscillator frequency $f_{\text{OSC}} = 6\,\text{MHz}$ for its clock source,

   (a) (4 pts) Find settings for $y =$ `PR2` and the $x =$ the `TMR2` Prescale Value which will produce as nearly as possible a pulse width modulation frequency $f_{\text{PWM}} = 1.4\,\text{kHz}$ from pulse width modulator number 2.
   SOLUTION:

   Because

   $$T_{\text{PWM}} = 4x(y+1)T_{\text{OSC}}$$

   so

   $$x(y+1) = \frac{f_{\text{OSC}}}{4f_{\text{PWM}}} = \frac{6\,\text{MHz}}{4(1.4\,\text{kHz})} = 1071.4.$$

   Because x must be in the set $\{1, 4, 16\}$, the only solution for this equation for which $y \leq 255$ is $\boxed{x = 16}$ and $\boxed{y = 65.96 \approx 66.}$

   (b) (4 pts) To four significant figures , what is the actual value of frequency f_{PWM} which results when $x = 4$ and $y = 250$?
   SOLUTION: The resultant pulse modulation frequency then is

   $$f_{\text{PWM}} = \frac{f_{\text{OSC}}}{4x(y+1)} = \frac{6\,\text{MHz}}{4(4)(250+1)} = \boxed{1.494\,\text{kHz.}}$$

   (c) (4 pts) To four significant figures, what is the relative error ρ_f in f_{PWM} when $f_{\text{PWM}} = 1.3\,\text{kHz}$?
   SOLUTION:

   $$\rho_f = \frac{f_{\text{ACHIEVED}} - f_{\text{DESIRED}}}{f_{\text{DESIRED}}} = \frac{1.3\,\text{kHz} - 1.4\,\text{kHz}}{1.4\,\text{kHz}} = \boxed{-7.143\%.}$$

(d) (4 pts) For the choice $x = 4$ and $y = 250$, find the contents of the 10-bit register $w =$ `CCPR2L:CCP2CON`$\langle 5{:}4 \rangle$ which most nearly achieves a duty cycle of $\eta = 38\%$.
SOLUTION: The modular output is high for time

$$T_{\text{H}} = wxT_{\text{OSC}}$$

and so the duty cycle is

$$\eta = \frac{T_{\text{H}}}{T_{\text{PWM}}} = \frac{wxT_{\text{OSC}}}{4x(y+1)T_{\text{OSC}}} = \frac{w}{4(y+1)} = \frac{w}{4(250+1)} = \frac{w}{1004}.$$

Therefore

$$w = 1004\,\eta = 1004(38\%) = \boxed{381.5 \approx 382.}$$

(e) (4 pts) To four decimals of accuracy, what is the actual duty cycle η which results when $x = 4$, $y = 250$, and $w = 400$?
SOLUTION:

$$\eta = \frac{w}{1004} = \frac{400}{1004} = \boxed{39.84\%.}$$

Register Address	Register Contents
01Eh	$3E_{16}$
09Eh	$C0_{16}$
01Fh	10010001_2
09Fh	00110000_2

Pin Number	Applied Voltage
2	3.5 V
3	2.7 V
4	1.5 V
5	4.5 V
6	3.7 V

Table 1: Register Contents and Pin Voltages

2. (32 pts) In the following questions assume that a PIC16F884 in the dual-inline package is being operated with a crystal clock source with frequency $f_{\text{OSC}} = 5\,\text{MHz}$. Just after the analog-to-digital converter has successfully completed the conversion of a voltage from an accelerometer sensor system, the register values and pin voltages shown in Table 1 apply. (Assume that the voltages given were stable throughout the conversion process.)

   (a) (4 pts) If the output impedance of the accelerometer sensor system is $R_{\text{S}} = 50\,\text{k}\Omega$, what is the converter's hold-capacitor charging time T_C? Give your answer to four significant figures.
   SOLUTION:

$$\begin{aligned} T_C &= -C_{\text{HOLD}}\,(R_{\text{IC}} + R_{\text{SS}} + R_{\text{S}})\ln(1/2047) \\ &= -10\,\text{pF}\,(1\,\text{k}\Omega + 7\,\text{k}\Omega + 50\,\text{k}\Omega)\ln(1/2047) \\ &= \boxed{4.422\ \mu\text{s.}} \end{aligned}$$

   (b) (4 pts) If $T_C = 15.00\,\mu\text{s}$ and if the ambient temperature is 50°C, then what is the total acquisition time T_{ACQ}? Give your answer to four significant figures.
   SOLUTION:

$$\begin{aligned} T_{\text{ACQ}} &= T_{\text{AMP}} + T_C + T_{\text{COFF}} \\ &= 2\,\mu\text{s} + 15\,\mu\text{s} + (50\,^\circ\text{C} - 25\,^\circ\text{C})(50\,\text{ns}/^\circ\text{C}) \\ &= \boxed{18.25\ \mu\text{s.}} \end{aligned}$$

   (c) (4 pts) What is the amount of time T_{CONV} required for a conversion? (T_{CONV} does not include the acquisition time T_{ACQ}.) Give your answer to four significant figures.
   SOLUTION: Because the `ADCON0` bits `ADCS1` and `ADCS0` are 1 and 0 respectively, $T_{\text{AD}} = 32 \times T_{\text{OSC}}$, so

$$T_{\text{CONV}} = 11T_{\text{AD}} + \frac{T_{\text{OSC}}}{2} = \frac{(11)(32)}{f_{\text{OSC}}} + \frac{1}{2\,f_{\text{OSC}}} = \frac{352.5}{5\,\text{MHz}} = \boxed{70.50\ \mu\text{s.}}$$

(d) (8 pts) It is necessary to wait for both the acquisition time and the conversion time to elapse every time we sample a voltage and convert it to its digital equivalent. With four analog inputs in use, each of similar frequency content and sampled equally often, what is the highest permissible frequency content of the sampled signals? Use the values $T_{\text{ACQ}} = 25\ \mu\text{s}$ and $T_{\text{CONV}} = 75\ \mu\text{s}$ and give your answer to four significant figures.

SOLUTION: The total time required to take a sample is

$$T_{\text{SAMPLE}} = T_{\text{ACQ}} + T_{\text{CONV}} = 25\ \mu\text{s} + 75\ \mu\text{s} = \boxed{100\ \mu\text{s.}}$$

For a single channel we need to take at least two such samples in each period of the highest frequency f_{MAX} present in any input. But with four inputs, we need to take a total of eight such samples in time T_{MAX}. Therefore

$$\begin{aligned} T_{\text{MAX}} &\geq 4 \times 2 \times T_{\text{SAMPLE}} \\ f_{\text{MAX}} &\leq \frac{1}{4 \times 2 \times T_{\text{SAMPLE}}} \\ &\leq \boxed{1.250\ \text{kHz.}} \end{aligned}$$

(e) (12 pts) On what pin of the PIC16F884 did the converted voltage v_{IN} appear? To four decimals of accuracy, give both the value of v_{IN} and the maximum ($\pm$) percentage error ϵ_{MAX} of this voltage?[1]

SOLUTION: The `CHS3:CHS0` bits (bits 5–2 of the `ADCON0` register at address 01Fh) are 0100_2, specifying channel 4. This is the `AN4` input on pin 7. Even though this voltage is not given, we can infer roughly what it must have been.

The `VCFG1:VCFG0` bits (bits 5 and 4 of the `ADCON1` register at address 09Fh) are 11_2, specifying that V_{REF}^{+} is obtained from `AN3` on pin 5, which is 4.5 V, and that V_{REF}^{-} is obtained from `AN2` on pin 4, which is 1.5 V.

The contents of `ADRESH` and `ADRESL` at addresses 01Eh and 09Fh constitute the 4-hexadecimal-digit number $3\text{EC}0_{16}$. The `ADFM` bit (bit 7 in the `ADCON1` register) is a 0, specifying that the 10-bit converted value D is left-justified in this 16-bit value, so it is $0\text{FB}_{16} = 251_{10}$. Therefore, the nominal input at pin 7 was

$$\begin{aligned} v_{\text{IN}} &= V_{\text{REF}}^{-} + \left(D + \frac{1}{2}\right)\frac{V_{\text{REF}}^{+} - V_{\text{REF}}^{-}}{2^{10}} \\ &= 1.5\ \text{V} + (251.5)\frac{4.5\ \text{V} - 1.5\ \text{V}}{2^{10}} \\ &= \boxed{2.237\ \text{V.}} \end{aligned}$$

The maximum error percentage would be one half of one quantum divided by the input voltage:

$$\begin{aligned} \epsilon_{\text{MAX}} &= \pm\left(\frac{V_{\text{REF}}^{+} - V_{\text{REF}}^{-}}{2 \cdot 2^{10}}\right)\left(\frac{1}{v_{\text{IN}}}\right) = \pm\left(\frac{4.5\ \text{V} - 1.5\ \text{V}}{2 \cdot 2^{10}}\right)\left(\frac{1}{2.237\ \text{V}}\right) \\ &= \boxed{\pm 0.06549\%.} \end{aligned}$$

[1] Assume that, for example, if voltage step 2 corresponds to any input from 1 V to 2 V, then the nominal input voltage must be 1.5 V.

3. (16 pts) The following questions apply to a PIC16F884-based system driven by an internal oscillator with frequency $f_{\text{OSC}} = 125\,\text{kHz}$.

   (a) (12 pts) Find choices for `BRGH` and `SPBRGH:SPBRG` or `SPBRG` to support asynchronous serial data transmission at a BAUD rate as near as it can possibly be to 9 kb/s. To four significant figures, what BAUD rate is achieved?

   SOLUTION: An expression for the BAUD rate is

$$f_{\text{BAUD}} = \frac{f_{\text{OSC}}}{m(n+1)}$$

   where

$$m \in \begin{cases} \{16, 4\} & \text{if BRGH= 1 and} \\ \{64, 16\} & \text{if BRGH= 0} \end{cases}$$

$$n = \begin{cases} \text{SPBRGH:SPBRG} & \text{if BR16= 1 and} \\ \text{SPBRG} & \text{if BR16= 0.} \end{cases}$$

   Solving for $m(n+1)$ yields

$$\begin{aligned} m(n+1) &= \frac{f_{\text{OSC}}}{f_{\text{BAUD}}} \\ &= \frac{125\,\text{kHz}}{9\,\text{kb/s}} \\ &= 13.9 \approx 14. \end{aligned}$$

   The only solutions that are even remotely close to this are

$$\begin{aligned} m &= 16, n = 0 \text{ and} \\ m &= \ \ 4, n = 2. \end{aligned}$$

   The resultant BAUD rates are

$$\begin{aligned} f_{\text{BAUD}} &= \frac{f_{\text{OSC}}}{m(n+1)} \\ &= \begin{cases} \frac{125\,\text{kHz}}{16(0+1)} & \text{if } m = 16, n = 0 \\ \frac{125\,\text{kHz}}{4(2+1)} & \text{if } m = 4, n = 2 \end{cases} \\ &= \begin{cases} 7.813\,\text{kHz} & \text{if } m = 16, n = 0 \\ 10.4\,\text{kHz} & \text{if } m = 4, n = 2. \end{cases} \end{aligned}$$

   Of these two solutions, the first is closer to the desired one of 9.0 kbps. It can be achieved either by picking

$$\boxed{\text{BRG16} = 1,\ \text{BRGH} = 0 \text{ and } \texttt{SPBRGH:SPBRG} = 0} \text{ or}$$

$$\boxed{\text{BRG16} = 0,\ \text{BRGH} = 1 \text{ and } \texttt{SPBRG} = 0.}$$

   In the second case, SPBRGH is not used. The resultant BAUD rate is $\boxed{7.813\,\text{kHz.}}$

(b) (4 pts) For an asynchronous serial eight-bit transmission with no parity bit, what is the effective throughput rate in bits per second (bps) if the achieved BAUD rate is 9.5 kHz? Give your answer to four significant figures.

SOLUTION: The efficiency is

$$\begin{aligned}\eta &= \frac{\text{Data bits}}{\text{All bits}} \\ &= \frac{8 \text{ data bits}}{1 \text{ start bit} + 8 \text{ data bits} + 1 \text{ stop bit}} \\ &= \boxed{80\,\%.}\end{aligned}$$

The throughput is

$$\begin{aligned}\tau &= \eta(\text{BAUD rate}) \\ &= (80\,\%)(9.5\,\text{kHz}) \\ &= 7.600\,\text{kbps}.\end{aligned}$$

4. (8 pts) A certain stepper motor can be controlled in both half-step and full-step modes. The angle associated with a whole step is 1°. A PIC16F884 operates the motor, issuing new output patterns (motor-coil activation signals) after some whole number of Timer 2 interrupts, which occur at 2 ms intervals.

   In attempting to achieve a rate of rotation of $n = 75$ rpm for this system, is it more accurate to issue whole steps or half steps? Use your answer to determine how many interrupts should be permitted to pass before issuing a new output pattern. To four significant figures, what rotation rate could you achieve that lies closest to this desired value? Explain your answers carefully.

   SOLUTION:

   We would like to get $75\,\text{rpm} \times \frac{1\,\text{min}}{60\,\text{s}} = 1.25\,\text{rev/s}$. This is equivalent to $450°/\text{s}$ and would require a new full step every $1/450\,\text{s} = 2.222\,\text{ms}$ or one new half step every 1.111 ms. Since the minimum interrupt interval of once every 2 ms is closer to the desired interval for whole steps, we should issue a new whole-step output pattern every interrupt.

   So one revolution takes

$$\begin{aligned} T_{\text{REV}} &= \frac{360\,\text{steps}}{\text{rev}} \times \frac{2\,\text{ms}}{\text{step}} \\ &= 720\,\text{ms/rev}, \end{aligned}$$

   which is equivalent to saying that the frequency f of rotation is

$$\begin{aligned} f &= \left(\frac{1\,\text{rev}}{720\,\text{ms}}\right)\left(\frac{60\,\text{s}}{\text{min}}\right) \\ f &= \boxed{83.33\,\text{rpm.}} \end{aligned}$$

5. (4 pts) If we decide to use analog comparator number 1 with an external voltage reference, four channels of analog inputs, and an external comparator output signal, which of the features of the PIC16F884 are still available?

   (a) Port A, Port C, and Timer 1 with an external input.

   (b) Port C, Timer 0 with an external input, and Timer 1 with an external input.

   (c) Port D, Timer 0 with an external input, and Timer 1 with an external input.

   (d) Port D, Timer 1 with an external input, and the EUSART.

Solution

The use of C12IN0−, C12IN1−, C1IN+, and C1OUT interferes with the use of some of the bits of Port A, so (a) is ruled out.

The use of C1IN+ inteferes with the use of Timer 0 with an external input, so (b) and (c) are ruled out.

The correct answer is $\boxed{\text{(d).}}$

6. (4 pts) Consider the arithmetic operation

$$\begin{array}{rl} & 1101\,1010 \\ + & 1011\,0000 \\ \hline \end{array}$$

Which of the following statements is correct?

(a) This causes overflow if the numbers are regarded as two's-complement numbers, but not if they are regarded as unsigned numbers.

(b) This does not cause overflow if the numbers are regarded as two's-complement numbers, but does so if they are regarded as unsigned numbers.

(c) This causes overflow if the numbers are regarded as two's-complement numbers, as it also does if they are regarded as unsigned numbers.

(d) This does not cause overflow if the numbers are regarded as two's-complement numbers, nor does it do so if they are regarded as unsigned numbers.

Solution

		Two's Complement	**Unsigned**
	1101 1010	-38_{10}	218_{10}
+	1011 0000	-80_{10}	176_{10}
$\boxed{\text{C}=1}$	1000 1010	-118_{10}	394_{10}

The carry bit is 1. If the numbers are unsigned, then this signifies an overflow, so only answers (b) and (c) could be right.

The two addends are negative numbers, and so is the result, if they are in two's-complement format. This means that there is no overflow, so the correct answer is $\boxed{\text{(b).}}$