From Concrete RTN to Control Signals: The Control Sequence

Tbl 4.6 The Instruction Fetch

Step	Concrete RTN	Control Sequence
T0	MA ← PC: C ← PC + 4;	PC_{out}, MA_{in}, INC4, C_{in}
T1	MD ← M[MA]: PC ← C;	Read, C_{out}, PC_{in}, Wait
T2	IR ← MD;	MD_{out}, IR_{in}
T3	Instruction_execution	

- The register transfers are the concrete RTN
- The control signals that cause the register transfers make up the control sequence
- Wait prevents the control from advancing to step T3 until the memory asserts Done

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Control Sequence for the SRC add Instruction

add (:= op = 12) → R[ra] ← R[rb] + R[rc]:

Tbl 4.7 The add Instruction

Step	Concrete RTN	Control Sequence
T0	MA ← PC: C ← PC + 4;	PC_{out}, MA_{in}, INC4, C_{in}, Read
T1	MD ← M[MA]: PC ← C;	C_{out}, PC_{in}, Wait
T2	IR ← MD;	MD_{out}, IR_{in}
T3	A ← R[rb];	Grb, R_{out}, A_{in}
T4	C ← A + R[rc];	Grc, R_{out}, ADD, C_{in}
T5	R[ra] ← C;	C_{out}, Gra, R_{in}, End

- Note the use of Gra, Grb, and Grc to gate the correct 5-bit register select code to the registers
- End signals the control to start over at step T0

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Control Sequence for the SRC addi Instruction

addi (:= op= 13) → R[ra] ← R[rb] + c2⟨16..0⟩ {2's comp., sign ext.} :

Tbl 4.8 The addi Instruction

Step	Concrete RTN	Control Sequence
T0.	MA ← PC: C ← PC + 4;	PC_{out}, MA_{in}, Inc4, C_{in}, Read
T1.	MD ← M[MA]; PC ← C;	C_{out}, PC_{in}, Wait
T2.	IR ← MD;	MD_{out}, IR_{in}
T3.	A ← R[rb];	Grb, R_{out}, A_{in}
T4.	C ← A + c2⟨16..0⟩ {sign ext.};	$c2_{out}$, ADD, C_{in}
T5.	R[ra] ← C;	C_{out}, Gra, R_{in}, End

- The $c2_{out}$ signal sign extends IR⟨16..0⟩ and gates it to the bus

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Control Sequence for the SRC st Instruction

st (:= op = 3) $\rightarrow$ M[disp] $\leftarrow$ R[ra] :
disp$\langle$31..0$\rangle$:= ((rb=0) $\rightarrow$ c2$\langle$16..0$\rangle$ {sign extend} :
(rb$\neq$0) $\rightarrow$ R[rb] + c2$\langle$16..0$\rangle$ {sign extend, 2's complement}) :

The st Instruction

Step	Concrete RTN	Control Sequence
T0–T2	Instruction fetch	Instruction fetch
T3	A $\leftarrow$ (rb=0) $\rightarrow$ 0: rb $\neq$ 0 $\rightarrow$ R[rb];	Grb, BA_{out}, A_{in}
T4	C $\leftarrow$ A + c2$\langle$16..0$\rangle$ {sign-extend};	$c2_{out}$, ADD, C_{in}
T5	MA $\leftarrow$ C;	C_{out}, MA_{in}
T6	MD $\leftarrow$ R[ra];	Gra, R_{out}, MD_{in}, Write
T7	M[MA] $\leftarrow$ MD;	Wait, End

- Note BA_{out} in T3 compared to R_{out} in T3 of addi

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Tbl 4.10 Control Sequence for the SRC shr Instruction—Looping

Step	Concrete RTN	Control Sequence
T0–T2	Instruction fetch	Instruction fetch
T3	$n \leftarrow IR\langle 4..0\rangle$;	$c1_{out}$, Ld
T4	$(n=0) \rightarrow (n \leftarrow R[rc]\langle 4..0\rangle)$;	$n=0 \rightarrow$ (Grc, R_{out}, Ld)
T5	$C \leftarrow R[rb]$;	Grb, R_{out}, C=B, C_{in}
T6	Shr (:= $(n\neq 0) \rightarrow$ ($C\langle 31..0\rangle \leftarrow 0\#C\langle 31..1\rangle$: $n \leftarrow n-1$; Shr));	$n\neq 0 \rightarrow$ (C_{out}, SHR, C_{in}, Decr, Goto6)
T7	$R[ra] \leftarrow C$;	C_{out}, Gra, R_{in}, End

- Conditional control signals and repeating a control step are new concepts

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Branching

$$
\begin{aligned}
\text{cond} := (\ & c3\langle 2..0\rangle = 0 \rightarrow 0: \\
& c3\langle 2..0\rangle = 1 \rightarrow 1: \\
& c3\langle 2..0\rangle = 2 \rightarrow R[rc] = 0: \\
& c3\langle 2..0\rangle = 3 \rightarrow R[rc] \neq 0: \\
& c3\langle 2..0\rangle = 4 \rightarrow R[rc]\langle 31\rangle = 0: \\
& c3\langle 2..0\rangle = 5 \rightarrow R[rc]\langle 31\rangle = 1\ ):
\end{aligned}
$$

- This is equivalent to the logic expression

$$
\begin{aligned}
\text{cond} = {} & (c3\langle 2..0\rangle = 1) \vee (c3\langle 2..0\rangle = 2) \wedge (R[rc] = 0) \vee \\
& (c3\langle 2..0\rangle = 3) \wedge \neg(R[rc] = 0) \vee (c3\langle 2..0\rangle = 4) \wedge \neg R[rc]\langle 31\rangle \vee \\
& (c3\langle 2..0\rangle = 5) \wedge R[rc]\langle 31\rangle
\end{aligned}
$$

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Tbl 4.11 Control Sequence for SRC Branch Instruction, br

br (:= op = 8) → (cond → PC ← R[rb]):

Step	Concrete RTN	Control Sequence
T0–T2	Instruction fetch	Instruction fetch
T3	CON ← cond(R[rc]);	Grc, R_{out}, CON_{in}
T4	CON → PC ← R[rb];	Grb, R_{out}, CON → PC_{in}, End

- Condition logic is always connected to CON, so R[rc] only needs to be put on bus in T3
- Only PC_{in} is conditional in T4 since gating R[rb] to bus makes no difference if it is not used

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