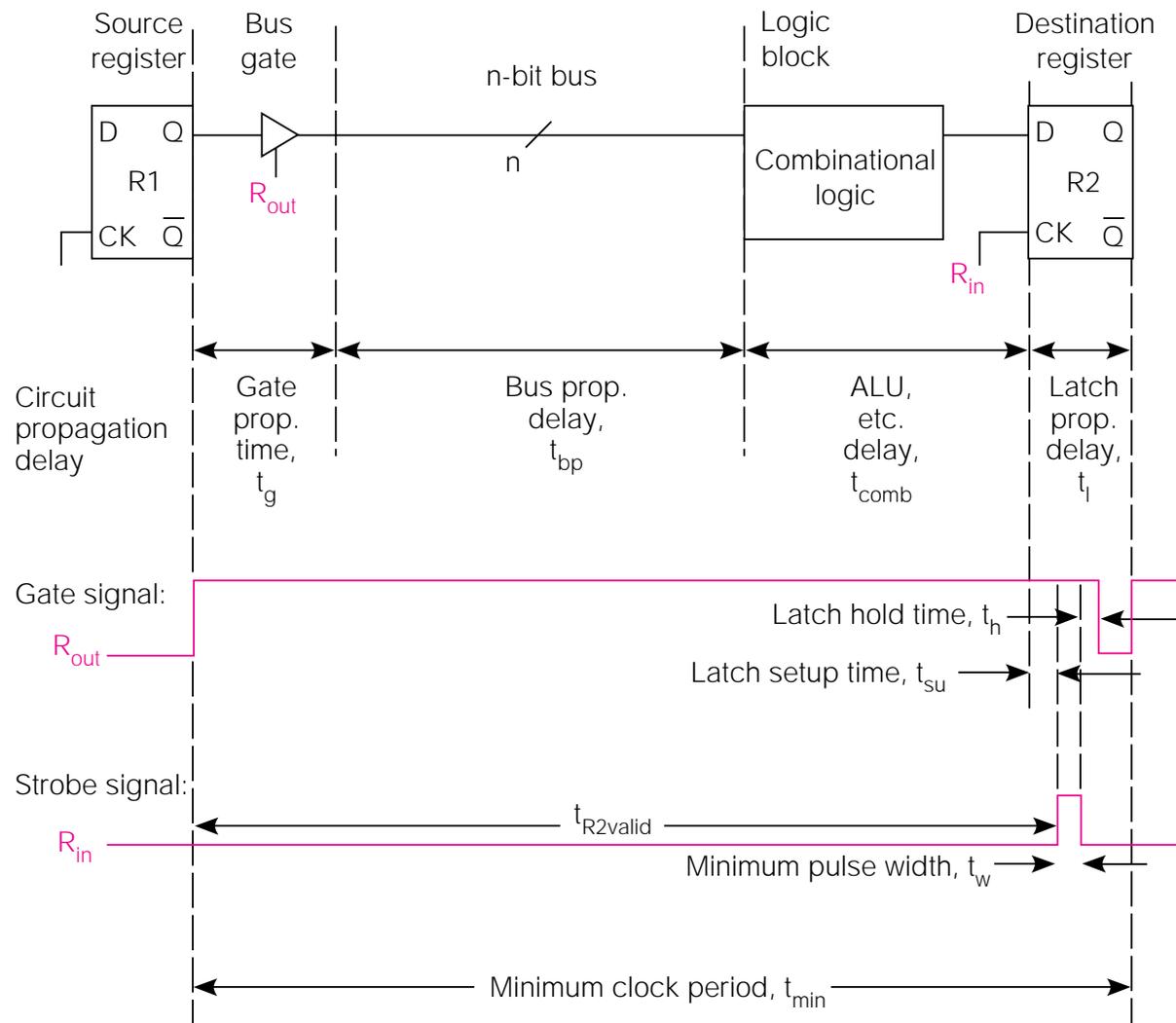


Fig 4.10 Clocking the Data Path: Register Transfer Timing



- **$t_{R2valid}$ is the period from begin of gate signal till inputs to R2 are valid**
- **t_{comb} is delay through combinational logic, such as ALU or cond logic**