

Tbl 4.13 The 2-Bus add Instruction

<u>Step</u>	<u>Concrete RTN</u>	<u>Control Sequence</u>
T0	$MA \leftarrow PC;$	$PC_{out}, C = B, MA_{in}, Read$
T1	$PC \leftarrow PC + 4; MD \leftarrow M[MA];$	$PC_{out}, INC4, PC_{in}, Wait$
T2	$IR \leftarrow MD;$	$MD_{out}, C = B, IR_{in}$
T3	$A \leftarrow R[rb];$	$Grb, R_{out}, C = B, A_{in}$
T4	$R[ra] \leftarrow A + R[rc];$	$Grc, R_{out}, ADD, Sra, R_{in}, End$

- Note the appearance of Grc to gate the output of the register rc onto the B bus and Sra to select ra to receive data strobed from the A bus
- Two register select decoders will be needed
- Transparent latches will be required at step T2