

Tbl 4.15 The 3-Bus add Instruction

<u>Step</u>	<u>Concrete RTN</u>	<u>Control Sequence</u>
T0	$MA \leftarrow PC; MD \leftarrow M[MA];$ $PC \leftarrow PC + 4;$	$PC_{out}, MA_{in}, INC4, PC_{in},$ Read, Wait
T1	$IR \leftarrow MD;$	$MD_{out}, C = B, IR_{in}$
T2	$R[ra] \leftarrow R[rb] + R[rc];$	$GArc, RA_{out}, GBrb, RB_{out},$ ADD, Sra, R_{in}, End

- Note the use of 3 register selection signals in step T2: $GArc$, $GBrb$, and Sra
- In step T0, PC moves to MA over bus B and goes through the ALU INC4 operation to reach PC again by way of bus C
 - PC must be edge-triggered or master-slave
- Once more MA must be a transparent latch