Tbl 4.17 The add Instruction with Reset Processing

Step	Concrete RTN
T0	$\neg$Rst $\rightarrow$(MA $\leftarrow$ PC: C $\leftarrow$ PC + 4):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$0):
T1	$\neg$Rst $\rightarrow$(MD $\leftarrow$ M[MA]: P $\leftarrow$ C):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$ 0):
T2	$\neg$Rst $\rightarrow$(IR $\leftarrow$ MD):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$ 0):
T3	$\neg$Rst $\rightarrow$(A $\leftarrow$ R[rb]):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$ 0):
T4	$\neg$Rst $\rightarrow$(C $\leftarrow$ A + R[rc]):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$ 0):
T5	$\neg$Rst $\rightarrow$ (R[ra] $\leftarrow$ C):
	Rst $\rightarrow$(Rst $\leftarrow$ 0: PC $\leftarrow$ 0: T $\leftarrow$ 0):

- See text for the corresponding control signals

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Control Sequences Including the Reset Function

Step	Control Sequence
T0	$\neg$Reset $\rightarrow$ (PC_{out}, MA_{in}, Inc4, C_{in}, Read):
	Reset $\rightarrow$ (ClrPC, ClrR, Goto0):
T1	$\neg$Reset $\rightarrow$ (C_{out}, PC_{in}, Wait):
	Reset $\rightarrow$ (ClrPC, ClrR, Goto0):
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- ClrPC clears the program counter to all zeros, and ClrR clears the 1-bit Reset flip-flop
- Because the same reset actions are in every step of every instruction, their control signals are independent of time step or opcode

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