

Synthesizing Control Signal Encoder Logic

Step Control Sequence

T0. PC_{out}' MA_{in}', Inc4, C_{in}', Read

T1. C_{out}' PC_{in}', Wait

T2. MD_{out}' IR_{in}

add		addi		st		shr	
<u>Step</u>	<u>Control Sequence</u>	<u>Step</u>	<u>Control Sequence</u>	<u>Step</u>	<u>Control Sequence</u>	<u>Step</u>	<u>Control Sequence</u>
T3.	Grb, R _{out} ' A _{in}	T3.	Grb, R _{out} ' A _{in}	T3.	Grb, BA _{out} ' A _{in}	T3.	c1 _{out} ' Ld
T4.	Grc, R _{out} ' ADD, C _{in}	T4.	c2 _{out} ' ADD, C _{in}	T4.	c2 _{out} ' ADD, C _{in}	T4.	n=0 → (Grc, R _{out} ' Ld)
T5.	C _{out} ' Gra , R _{in} ', End	T5.	C _{out} ' Gra , R _{in} ', End	T5.	C _{out} ' MA _{in}	T5.	Grb, R _{out} ' C=B
				T6.	Gra , R _{out} ' MD _{in} ', Write	T6.	n≠0 → (C _{out} ' SHR, C _{in} ', Decr, Goto7)
				T7.	Wait, End	T7.	C _{out} ' Gra , R _{in} ', End

Design process:

- Comb through the entire set of control sequences.
- Find all occurrences of each control signal.
- Write an equation describing that signal.

Example: Gra = T5·(add + addi) + T6·st + T7·shr + ...

Fig 4.12 Generation of the logic for PC_{in} and G_{ra}

