

EC362 Lab #3

VHDL ALU Design

The objective of this laboratory is to provide you with experience in specifying behavioral and structural VHDL descriptions of familiar components, all with the goal of producing a 16 bit 5 function ALU.

Lab part 1: Develop a behavioral VHDL model for a 2x16 multiplexer (MUX). Develop a test bench for your model that demonstrates basic functionality.

Lab part 2: Develop a behavioral VHDL model for a 4x16 multiplexer (MUX). Develop a test bench for your model that demonstrates basic functionality.

Lab part 3: Develop a behavioral/structural VHDL model for a 16-bit full adder (FA). Your model should also provide a special 1 bit "Overflow Detect" output signal. Develop a test bench for your model that demonstrates basic functionality. You may find it useful to develop this hierarchically by designing a 1 bit full adder first, then instantiating four of these to create a 4 bit full adder, and then instantiate four of these also to create a 16 bit full adder.

Lab part 4: Develop a structural VHDL model that uses your models from parts 1, 2, and 3 to implement a 16-bit ALU that implements the following control functions:

C2	C1	C0	Function
0	0	0	And
0	0	1	Or
0	1	0	Add
0	1	1	Sub
1	1	1	Set-on-less-than