

EC362 Lab #4

VHDL ALU Design (continued)

This laboratory is a continuation of lab #3 in which you were to design a 16 bit 5 function ALU. The four parts of that lab were to:

Part 1: Develop a behavioral VHDL model for a 2x16 multiplexer (MUX).

Part 2: Develop a behavioral VHDL model for a 4x16 multiplexer (MUX).

Part 3: Develop a behavioral/structural VHDL model for a 16-bit full adder (FA) with a 1 bit “Overflow Detect” output signal.

Part 4: Develop a structural VHDL model that uses your models from parts 1, 2, and 3 to implement a 16-bit ALU that implements the following control functions:

C2	C1	C0	Function
0	0	0	And
0	0	1	Or
0	1	0	Add
0	1	1	Sub
1	1	1	Set-on-less-than

(NEW) Part 5: In this lab, you should continue the design above, but replace the ripple carry adder you designed in part 3 with a carry-lookahead adder. In this instance, you may design the adder circuit using any style you prefer – behavioral or structural. Develop a test bench for your model that demonstrates basic functionality.