

EC362 Lab #5

VHDL Register File Design

The objective of this laboratory is to design a register file that consists of 16 registers (numbered 0 to 15) each consisting of 16 bits. The register file should consist of two 16 bit output ports (for reading two registers simultaneously) and one 16 bit input port (for writing data into a register), and any other necessary ports or control signals required to properly control the register file.

I have created some templates to help guide your work. You should start with those and fill in the details – all are located on the website. One of the files is a special “library” file called mylibrary.vhd. You will want to download that to your local computer and include it in every project in which you wish to use the special type that I have created.

Part 1: Develop a behavioral VHDL model for a 16x16 multiplexer (MUX). Develop a test bench for your model that demonstrates basic functionality.

Part 2: Develop a behavioral VHDL model for a 4 to 16 decoder. Develop a test bench for your model that demonstrates basic functionality.

Part 3: Develop a behavioral/structural VHDL model for the register file. You will need to instantiate sixteen of the 16-bit registers, two of the 16x16 MUXes and one 4 to 16 decoder. Consider using the VHDL “generate” construct to create the needed port mappings for the registers. Develop a test bench for your model that demonstrates basic functionality.